[ICITEE 2016] Your paper #1570292305 ('Comparison of Three F Unbalanced Grid Voltage Conditions')

Inbox x

icitee2016-chairs@edas.info
to me, Mochammad, Ardyono, Mauridhi

Dear Mr. Iwan Setiawan:

Congratulations - your paper #1570292305 ('Comparison of Three Popular PLL Conditions') has been accepted for presentation in ICITEE 2016, and will be pu that only PRESENTED PAPERS will be submitted to IEEEXplore.

Please reflect the reviewers' comments into your final manuscript, the detail revi php?m=1570292305, using your EDAS login name setiaone.iwan@gmail.com.

Please also consider 4 mandatory steps for author in submitting the camera-rea

1. REGISTRATION AND PAYMENT

Please be reminded that the due date for early bird registration is 10 August 201 At least one author has to register for the conference. Note that the Gala Dinner Payment and registration details can be found at:

https://edas.info/r22473 (for International participants)
http://icitee.ugm.ac.id/new/registration-2/ (for International and National participa

After payment, please complete the registration confirmation at:
(i) For presenter:
http://icitee.ugm.ac.id/new/registration-confirmation-for-presenter/

(ii) For participant non-presenter:
http://icitee.ugm.ac.id/new/registration-confirmation-for-non-presenter/

(1570292305): *COMPARISON OF THREE POPULAR PLL SCHEMES UNDER BALANCED AND UNBALANCED GRID VOLTAGE CONDITIONS*

Response to Reviewer

Dear Reviewers

We would like to thank you for your valuable comments that helped us to improve our paper. Please find below our detailed reply to your comments.

Sincerely yours,

Iwan Setiawan et al.

Comments of Reviewer #B

The use of capital letters in the acronym that of the sentence is wrong. Supposedly: phase lock loop (PLL), a positive-negative sequence calculator (PNSC). There are still some typing errors eg capital letters in the sentence or small letters at the beginning of the sentence. Acknowledgment is not yet complete. The format of writing a bibliography is not as consistent as the format of writing. Is there a novelty of this study?

Authors' Response:

Thank you for your reminder and your suggestions. We have rechecked the manuscript carefully and revised the typos, the acronym and tried to avoid any grammar error or syntax error. We also have completed the Acknowledgment. For the bibliography, we here used the format under paper templete. Due this work is just comparative study, to be frank with you this study lacks novelty.

Comments of Reviewer #C

1. ... Although there are many PLL topologies which are proposed in literatures[11-13], however in practice only a few which relatively popular due to theirs strength. --> what is theirs strength mean?

2. some texts in the pictures are very small to see, please make it bigger.

Authors' Response:

1. Thank you for your reminder. In this study, two criterias that we used to determine PLLs under study: simplicity in structure and its perpormance. To be more clear, we have changed the previous statement to be:

.....Although there are many PLL topologies which are proposed in literatures[11-13], however in practice only a few which popular due to their relatively simple structure and their performances

2. Thank you for your suggestion. In the revised manuscript we have made the texts larger in some picture (Fig.1-Fig.9). So now, the texts are more clearer.

Comments of Reviewer #D

1. Please recheck the reference style errors.

2. Please justify why do we need this comparative study in the introduction

Authors' Response:

1. Thank you for your reminder. In the revised manuscript, we have corrected the reference style errors

Manuscript ID 8387

Paper Title : Control Strategy based on Associative Memory Networks for a Grid-Side Converter in On-Grid Renewable Generation Systems under Generalized Unbalanced Grid Voltage Conditions

2. Thank you for your suggestion. In the revised manuscript we have justified the importance of this study that placed in Introduction Section as follow:

The aims of this paper is to investigate of several most popular PLLs: Synchronous reference frame-phase locked loop (SRF-PLL), dicouple double synchronous reference frame-phase locked loop (DDSRF-PLL) and dicouple double second order general integrator-phase locked loop (DSOGI-PLL) in response to the grid voltage magnitude changes, both symetrical and asymetrical changes. By this study, the appropriate PLL topology can be chosen based on the GCS controller requirement.