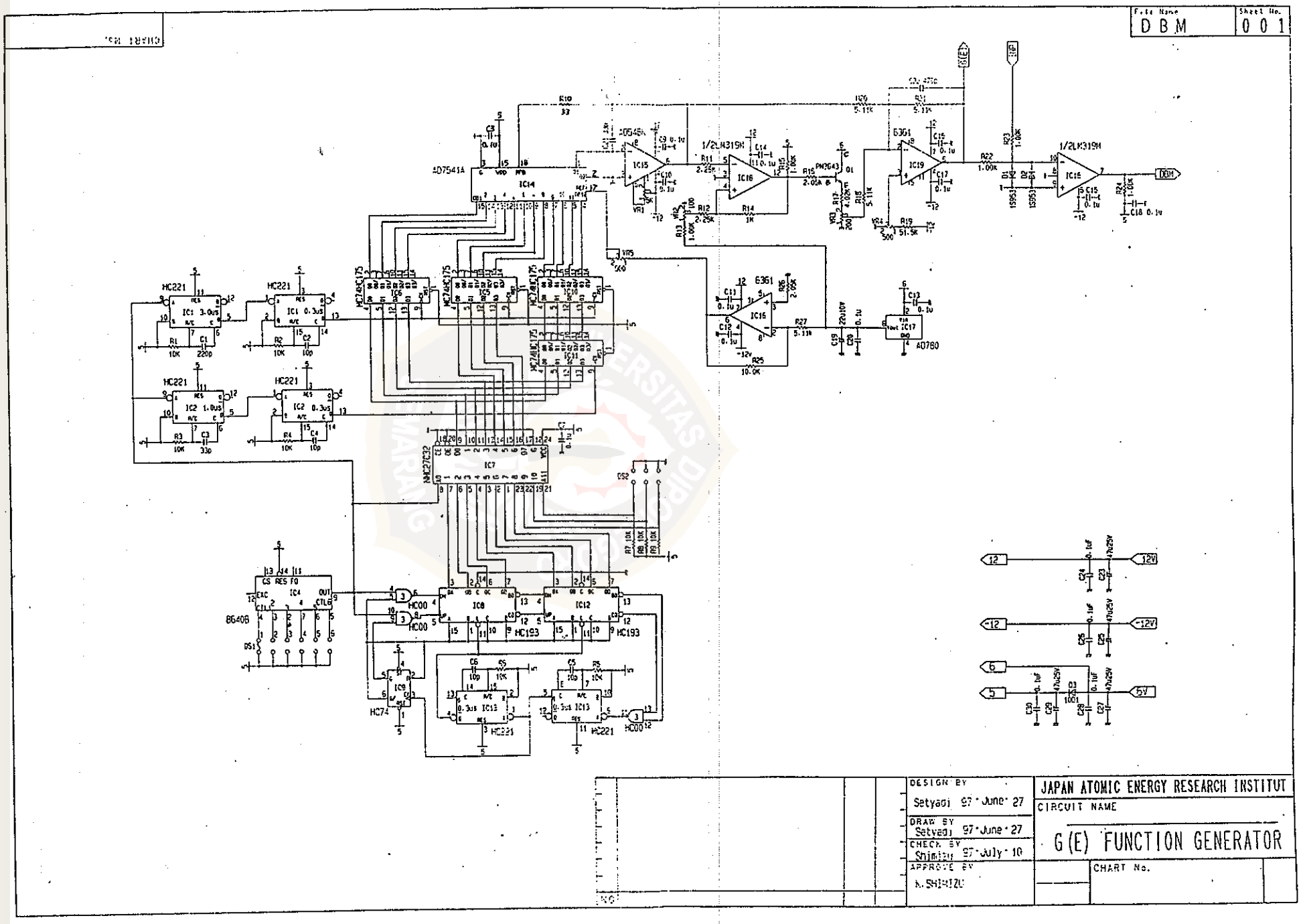
Lampiran A

Rangkaian Generator G(E)



Lampiran B

G(E) DATA for 2"x2" NaI(Tl) Scintillation Detector

Lampiran G(E) DATA for 2"X2"NaI(Tl) Scintillation detector

Channel No.	Passing Rate [%]	G(E) Value [uR/h/cpm*10E-2]	Energy [KeV]	EPROM DATA Decimal	EPROM DATA Hex-Decimal
0	100.000	0.88620	3000	4095	FFF
1	99.609	0.88274	2980	4068	FE3
2	99.219	0.87928	2960	4040	FC8
3	98.828	0.87581	2940	4013	FAD
4	98.438	0.87235	2920	3986	F91
5	98.047	0.86889	2900	3959	F76
6	97.656	0.86543	2880	3931	F5B
7	97.266	0.86197	2860	3904	F3F
8	96.875	0.85851	2835	3870	F1D
9	96.484	0.85504	2815	3842	F02
10	96.094	0.85158	2795	3815	EE7
11	95.703	0.84812	2775	3788	ECB
12	95.313	0.84466	2755	3761	EB0
13	94.922	0.84120	2730	3726	E8E
14	94.531	0.83774	2710	3699	E73
15	94.141	0.83427	2690	3672	E57
16	93.750	0.83081	2665	3638	E35
17	93.359	0.82735	2645	3610	E1A
18	92.969	0.82389	2625	3583	DFF
19	92.578	0.82043	2600	3549	DDD
20	92.188	0.81697	2580	3522	DC1
21	91.797	0.81350	2560	3494	DA6
22	91.406	0.81004	2535	3460	D84
23	91.016	0.80658	2515	3433	D68
24	90.625	0.80312	2495	3406	D4D
25	90.234	0.79966	2470	3372	D2B
26	89.844	0.79620	2450	3344	D10
27	89.453	0.79273	2430	3317	CF4
28	89.063	0.78927	2410	3290	CD9
29	88.672	0.78581	2385	3256	CB7
30	88.281	0.78235	2365	3228	C9C
31	87.891	0.77889	2345	3201	C80
32	87.500	0.77543	2320	3167	C5E
33	87.109	0.77196	2300	3140	C43
34	86.719	0.76850	2280	3112	C28
35	86.328	0.76504	2260	3085	C0C
36	85.938	0.76158	2240	3058	BF1
37	85.547	0.75812	2220	3030	BD6
38	85.156	0.75465	2200	3003	BBB
39	84.766	0.75119	2180	2976	B9F
40	84.375	0.74773	2160	2948	B84
41	83.984	0.74427	2150	2935	B76
42	83.594	0.74081	2120	2894	B4D
43	83.203	0.73735	2100	2867	B32
44	82.813	0.73388	2080	2839	B17
45	82.422	0.73042	2060	2812	AFB
46	82.031	0.72696	2045	2791	AE7
47	81.641	0.72350	2025	2764	ACC
48	81.250	0.72004	2005	2737	AB0
49	80.859	0.71658	1990	2716	A9C
50	80.469	0.71311	1970	2689	A81
51	80.078	0.70965	1955	2669	A6C
52	79.688	0.70619	1935	2641	A51
53	79.297	0.70273	1920	2621	A3C

G(E) DATA for 2"X2"NaI(Tl) Scintillation detector

54	78.906	0.69927	1900	2594	A21
55	78.516	0.69581	1885	2573	A0D
56	78.125	0.69234	1865	2546	9F1
57	77.734	0.68888	1850	2525	9DD
58	77.344	0.68542	1835	2505	9C8
59	76.953	0.68196	1820	2484	9B4
60	76.563	0.67850	1805	2464	99F
61	76.172	0.67504	1785	2437	984
62	75.781	0.67157	1770	2416	970
63	75.391	0.66811	1755	2396	95B
64	75.000	0.66465	1740	2375	947
65	74.609	0.66119	1725	2355	932
66	74.219	0.65773	1715	2341	924
67	73.828	0.65426	1700	2321	910
68	73.438	0.65080	1685	2300	8FC
69	73.047	0.64734	1670	2280	8E7
70	72.656	0.64388	1655	2259	8D3
71	72.266	0.64042	1640	2239	8BE
72	71.875	0.63696	1630	2225	8B0
73	71.484	0.63349	1615	2204	89C
74	71.094	0.63003	1600	2184	888
75	70.703	0.62657	1590	2170	87A
76	70.313	0.62311	1575	2150	865
77	69.922	0.61965	1565	2136	858
78	69.531	0.61619	1550	2116	843
79	69.141	0.61272	1540	2102	836
80	68.750	0.60926	1525	2082	821
81	68.359	0.60580	1515	2068	813
82	67.969	0.60234	1500	2048	7FF
83	67.578	0.59888	1490	2034	7F1
84	67.188	0.59542	1480	2020	7E4
85	66.797	0.59195	1465	2000	7CF
86	66.406	0.58849	1455	1986	7C2
87	66.016	0.58503	1445	1972	7B4
88	65.625	0.58157	1430	1952	79F
89	65.234	0.57811	1420	1938	792
90	64.844	0.57465	1410	1925	784
91	64.453	0.57118	1400	1911	777
92	64.063	0.56772	1390	1897	769
93	63.672	0.56426	1380	1884	75B
94	63.281	0.56080	1370	1870	74E
95	62.891	0.55734	1355	1850	739
96	62.500	0.55388	1345	1836	72B
97	62.109	0.55041	1335	1822	71E
98	61.719	0.54695	1325	1809	710
99	61.328	0.54349	1315	1795	702
100	60.938	0.54003	1305	1781	6F5
101	60.547	0.53657	1295	1768	6E7
102	60.156	0.53310	1285	1754	6DA
103	59.766	0.52964	1275	1740	6CC
104	59.375	0.52618	1270	1734	6C5
105	58.984	0.52272	1260	1720	6B7
106	58.594	0.51926	1250	1706	6AA
107	58.203	0.51580	1240	1693	69C
108	57.813	0.51233	1230	1679	68E
109	57.422	0.50887	1220	1665	681

G(E) DATA for 2"X2"NaI(Tl) Scintillation detector

110	57.031	0.50541	1210	1652	673
111	56.641	0.50195	1205	1645	66C
112	56.250	0.49849	1195	1631	65F
113	55.859	0.49503	1185	1618	651
114	55.469	0.49156	1175	1604	643
115	55.078	0.48810	1170	1597	63D
116	54.688	0.48464	1160	1583	62F
117	54.297	0.48118	1150	1570	621
118	53.906	0.47772	1140	1556	614
119	53.516	0.47426	1135	1549	60D
120	53.125	0.47079	1125	1536	5FF
121	52.734	0.46733	1115	1522	5F1
122	52.344	0.46387	1110	1515	5EB
123	51.953	0.46041	1100	1502	5DD
124	51.563	0.45695	1090	1488	5CF
125	51.172	0.45349	1085	1481	5C9
126	50.781	0.45002	1075	1467	5BB
127	50.391	0.44656	1065	1454	5AD
128	50.000	0.44310	1060	1447	5A6
129	49.609	0.43964	1055	1440	5A0
130	49.219	0.43618	1045	1426	592
131	48.828	0.43271	1035	1413	584
132	48.438	0.42925	1030	1406	57D
133	48.047	0.42579	1020	1392	570
134	47.656	0.42233	1015	1385	569
135	47.266	0.41887	1005	1372	55B
136	46.875	0.41541	1000	1365	555
137	46.484	0.41194	990	1351	547
138	46.094	0.40848	985	1345	540
139	45.703	0.40502	975	1331	532
140	45.313	0.40156	970	1324	52C
141	44.922	0.39810	965	1317	525
142	44.531	0.39464	955	1304	517
143	44.141	0.39117	950	1297	510
144	43.750	0.38771	940	1283	503
145	43.359	0.38425	935	1276	4FC
146	42.969	0.38079	925	1263	4EE
147	42.578	0.37733	920	1256	4E7
148	42.188	0.37387	915	1249	4E0
149	41.797	0.37040	905	1235	4D3
150	41.406	0.36694	900	1229	4CC
151	41.016	0.36348	890	1215	4BE
152	40.625	0.36002	885	1208	4B8
153	40.234	0.35656	880	1201	4B1
154	39.844	0.35310	870	1188	4A3
155	39.453	0.34963	865	1181	49C
156	39.063	0.34617	860	1174	495
157	38.672	0.34271	850	1160	488
158	38.281	0.33925	845	1153	481
159	37.891	0.33579	840	1147	47A
160	37.500	0.33233	830	1133	46C
161	37.109	0.32886	825	1126	466
162	36.719	0.32540	820	1119	45F
163	36.328	0.32194	810	1106	451
164	35.938	0.31848	805	1099	44A
165	35.547	0.31502	800	1092	444

G(E) DATA for 2"X2"NaI(Tl) Scintillation detector

166	35.156	0.31155	790	1078	436
167	34.766	0.30809	785	1072	42F
168	34.375	0.30463	780	1065	428
169	33.984	0.30117	775	1058	421
170	33.594	0.29771	765	1044	414
171	33.203	0.29425	760	1037	40D
172	32.813	0.29078	755	1031	406
173	32.422	0.28732	745	1017	3F8
174	32.031	0.28386	740	1010	3F2
175	31.641	0.28040	735	1003	3EB
176	31.250	0.27694	730	996	3E4
177	30.859	0.27348	720	983	3D6
178	30.469	0.27001	715	976	3CF
179	30.078	0.26655	710	969	3C9
180	29.688	0.26309	705	962	3C2
181	29.297	0.25963	695	949	3B4
182	28.906	0.25617	690	942	3AD
183	28.516	0.25271	685	935	3A7
184	28.125	0.24924	680	928	3A0
185	27.734	0.24578	670	915	392
186	27.344	0.24232	665	908	38B
187	26.953	0.23886	660	901	384
188	26.563	0.23540	655	894	37E
189	26.172	0.23194	645	880	370
190	25.781	0.22847	640	874	369
191	25.391	0.22501	635	867	362
192	25.000	0.22155	630	860	35B
193	24.609	0.21809	625	853	355
194	24.219	0.21463	615	839	347
195	23.828	0.21116	610	833	340
196	23.438	0.20770	605	826	339
197	23.047	0.20424	600	819	333
198	22.656	0.20078	590	805	325
199	22.266	0.19732	585	799	31E
200	21.875	0.19386	580	792	317
201	21.484	0.19039	575	785	310
202	21.094	0.18693	570	778	30A
203	20.703	0.18347	560	764	2FC
204	20.313	0.18001	555	758	2F5
205	19.922	0.17655	550	751	2EE
206	19.531	0.17309	545	744	2E7
207	19.141	0.16962	535	730	2DA
208	18.750	0.16616	530	723	2D3
209	18.359	0.16270	525	717	2CC
210	17.969	0.15924	515	703	2BE
211	17.578	0.15578	510	696	2B8
212	17.188	0.15232	505	689	2B1
213	16.797	0.14885	500	683	2AA
214	16.406	0.14539	490	669	29C
215	16.016	0.14193	485	662	296
216	15.625	0.13847	480	655	28F
217	15.234	0.13501	470	642	281
218	14.844	0.13155	465	635	27A
219	14.453	0.12808	460	628	273
220	14.063	0.12462	450	614	266
221	13.672	0.12116	445	607	25F

G(E) DATA for 2"X2"NaI(Tl) Scintillation detector

222	13.281	0.11770	440	601	258
223	12.891	0.11424	430	587	24A
224	12.500	0.11078	425	580	244
225	12.109	0.10731	415	566	236
226	11.719	0.10385	410	560	22F
227	11.328	0.10039	400	546	222
228	10.938	0.09693	395	539	21B
229	10.547	0.09347	390	532	214
230	10.156	0.09000	380	519	206
231	9.766	0.08654	370	505	1F9
232	9.375	0.08308	365	498	1F2
233	8.984	0.07962	355	485	1E4
234	8.594	0.07616	350	478	1DD
235	8.203	0.07270	340	464	1D0
236	7.813	0.06923	330	450	1C2
237	7.422	0.06577	320	437	1B4
238	7.031	0.06231	310	423	1A7
239	6.641	0.05885	300	410	199
240	6.250	0.05539	290	396	18B
241	5.859	0.05193	280	382	17E
242	5.469	0.04846	270	369	170
243	5.078	0.04500	260	355	162
244	4.688	0.04154	245	334	14E
245	4.297	0.03808	235	321	140
246	3.906	0.03462	220	300	12C
247	3.516	0.03116	205	280	117
248	3.125	0.02769	190	259	103
249	2.734	0.02423	170	232	E8
250	2.344	0.02077	150	205	CC
251	1.953	0.01731	130	177	B1
252	1.563	0.01385	110	150	96
253	1.172	0.01039	90	123	7A
254	0.781	0.00692	90	123	7A
255	0.391	0.00346	90	123	7A

Lampiran C

Data Karakteristik Komponen

Lampiran C.1. Data Karakteristik EPROM 2732

GENERAL DESCRIPTION

4096-word × 8-bit U. V. Erasable and Programmable Read Only Memory

The 2732A is a 4096-word by 8-bit erasable and electrically programmable ROM. This device is packaged in a 24 pin dual-in-line package with transparent lid.
The transparent lid on the package allow the memory content to be erased with ultraviolet light.

FEATURES

- Single Power Supply ..... +5V ±5%
- Simple Programming Program Voltage: +21V D.C
  Program with one 50ms Pulse
- Static ..... No clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Mode

- Absolute Max. Rating of V_{PP} Pin..... 26.5V
- Low Stand-by Current ..... 35mA (max)

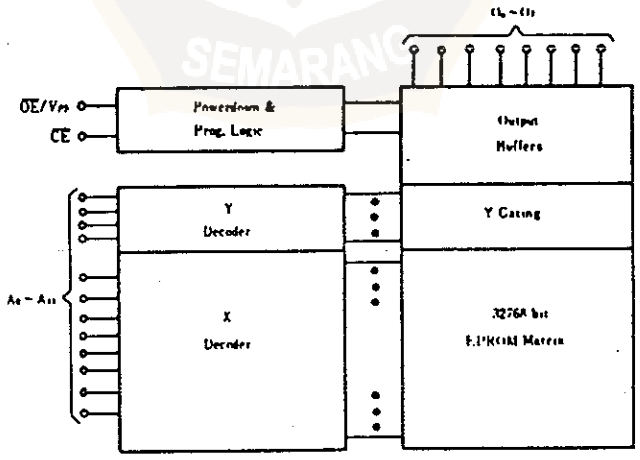
PIN CONNECTION

(Top View)

MODE SELECTION

Pins / MODE	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	Outputs (9~11, 13~17)
Read	V_{IL}	V_{IL}	+5	Dout
Stand by	V_{IH}	Don't Care	+5	High Z
Program	V_{IL}	V_{PP}	+5	Din
Program Verify	V_{IL}	V_{IL}	+5	Dout
Program Inhibit	V_{IH}	V_{PP}	+5	High Z

BLOCK DIAGRAM



ANALOG DEVICES

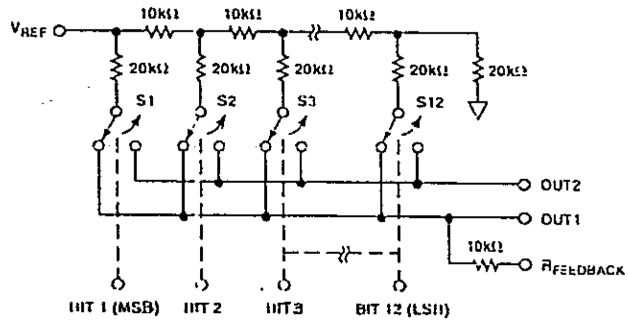
CMOS 12-Bit Monolithic Multiplying DAC

AD7541A

FEATURES

Improved Version of AD7541
Full Four-Quadrant Multiplication
12-Bit Linearity (Endpoint)
All Parts Guaranteed Monotonic
TTL/CMOS Compatible
Low Cost
Protection Schottky Diodes Not Required
Low Logic Input Leakage

FUNCTIONAL BLOCK DIAGRAM



DIGITAL INPUTS (DTL/TTL/CMOS COMPATIBLE)

LOGIC: A SWITCH IS CLOSED TO I_{OUT1} FOR ITS DIGITAL INPUT IN A "HIGH" STATE.

GENERAL DESCRIPTION

The Analog Devices AD7541A is a low cost, high performance 12-bit monolithic multiplying digital-to-analog converter. It is fabricated using advanced, low noise, thin film on CMOS technology and is available in a standard 18-lead DIP and in 20-terminal surface mount packages.

The AD7541A is functionally and pin compatible with the industry standard AD7541 device and offers improved specifications and performance. The improved design ensures that the device is latch-up free so no output protection Schottky diodes are required.

This new device uses laser wafer trimming to provide full 12-bit endpoint linearity with several new high performance grades.

ORDERING GUIDE[1]

Model[2]	Temperature Range	Relative Accuracy T_{MIN} to T_{MAX}	Gain Error $T_A = +25°C$	Package Options[3]
AD7541AJN	0°C to +70°C	±1 LSB	±6 LSB	N-18
AD7541AKN	0°C to +70°C	±1/2 LSB	±1 LSB	N-18
AD7541AJP	0°C to +70°C	±1 LSB	±6	P-20A
AD7541AKP	0°C to +70°C	±1/2 LSB	±1	P-20A
AD7541AKR	0°C to +70°C	±1/2 LSB	±1	R-18
AD7541AAQ	–25°C to +85°C	±1 LSB	±6 LSB	Q-18
AD7541ABQ	–25°C to +85°C	±1/2 LSB	±1 LSB	Q-18
AD7541ASQ	–55°C to +125°C	±1 LSB	±6 LSB	Q-18
AD7541ATQ	–55°C to +125°C	±1/2 LSB	±1 LSB	Q-18
AD7541ASE	–55°C to +125°C	±1 LSB	±6 LSB	E-20A
AD7541ATE	–55°C to +125°C	±1/2 LSB	±1 LSB	E-20A

NOTES
[1]Analog Devices reserves the right to ship either ceramic (D-18) or cerdip (Q-18) hermetic packages.
[2]To order MIL-STD-883, Class B process parts, add /883B to part number. Contact local sales office for military data sheet.
[3]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = Small Outline IC.

PRODUCT HIGHLIGHTS

Compatibility: The AD7541A can be used as a direct replacement for any AD7541-type device. As with the Analog Devices AD7541, the digital inputs are TTL/CMOS compatible and have been designed to have a ±1 µA maximum input current requirement so as not to load the driving circuitry.

Improvements: The AD7541A offers the following improved specifications over the AD7541:

1. Gain Error for all grades has been reduced with premium grade versions having a maximum gain error of ±3 LSB.
2. Gain Error temperature coefficient has been reduced to 2 ppm/°C typical and 5 ppm/°C maximum.
3. Digital-to-analog charge injection energy for this new device is typically 20% less than the standard AD7541 part.
4. Latch-up proof.
5. Improvements in laser wafer trimming provides 1/2 LSB max differential nonlinearity for top grade devices over the operating temperature range (vs. 1 LSB on older 7541 types).
6. All grades are guaranteed monotonic to 12 bits over the operating temperature range.

REV. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 World Wide Web Site: http://www.analog.com
Fax: 617/326-8703

AD7541A—SPECIFICATIONS (V_{DD} = +15 V, V_{REF} = +10 V; OUT 1 = OUT 2 = GND = 0 V unless otherwise noted)

Parameter	Version	T_A = +25°C	T_A = T_{MIN}, T_{MAX}[1]	Units	Test Conditions/Comments
ACCURACY					
Resolution	All	12	12	Bits	
Relative Accuracy	J, A, S	±1	±1	LSB max	±1 LSB = ±0.024% of Full Scale
	K, B, T	±1/2	±1/2	LSB max	±1/2 LSB = ±0.012% of Full Scale
Differential Nonlinearity	J, A, S	±1	±1	LSB max	All Grades Guaranteed Monotonic
	K, B, T	±1/2	±1/2	LSB max	to 12 Bits, T_{MIN} to T_{MAX}.
Gain Error	J, A, S	±6	±8	LSB max	Measured Using Internal R_{FB} and Includes
	K, B, T	±3	±5	LSB max	Effect of Leakage Current and Gain TC.
					Gain Error Can Be Trimmed to Zero.
Gain Temperature Coefficient[2]					
ΔGain/ΔTemperature	All	5	5	ppm/°C max	Typical Value Is 2 ppm/°C.
Output Leakage Current					
OUT1 (Pin 1)	J, K	±5	±10	nA max	All Digital Inputs = 0 V.
	A, B	±5	±10	nA max	
	S, T	±5	±200	nA max	
OUT2 (Pin 2)	J, K	±5	±10	nA max	All Digital Inputs = V_{DD}.
	A, B	±5	±10	nA max	
	S, T	±5	±200	nA max	
FERENCE INPUT					
Input Resistance (Pin 17 to GND)	All	7–18	7–18	kΩ min/max	Typical Input Resistance = 11 kΩ.
					Typical Input Resistance Temperature
					Coefficient = −300 ppm/°C.
DIGITAL INPUTS					
V_{IH} (Input HIGH Voltage)	All	2.4	2.4	V min	
V_{IL} (Input LOW Voltage)	All	0.8	0.8	V max	
I_{IN} (Input Current)	All	±1	±1	μA max	Logic Inputs Are MOS Gates. I_{IN} typ (25°C) = 1 n
C_{IN} (Input Capacitance)[2]	All	8	8	pF max	V_{IN} = 0 V
POWER SUPPLY REJECTION					
ΔGain/ΔV_{DD}	All	±0.01	±0.02	% per % max	ΔV_{DD} = ±5%
POWER SUPPLY					
V_{DD} Range	All	+5 to +16	+5 to +16	V min/V max	Accuracy Is Not Guaranteed Over This Range.
I_{DD}	All	2	2	mA max	All Digital Inputs V_{IL} or V_{IH}.
		100	500	μA max	All Digital Inputs 0 V or V_{DD}.

AC PERFORMANCE CHARACTERISTICS

These Characteristics are included for Design Guidance only and are not subject to test. V_{DD} = +15 V, V_{IR} = +10 V except where noted, OUT1 = OUT2 = GND = 0 V, Output Amp is AD544 except where noted.

Parameter	Version[1]	T_A = +25°C	T_A = T_{MIN}, T_{MAX}[1]	Units	Test Conditions/Comments
PROPAGATION DELAY (From Digital Input Change to 90% of Final Analog-Output)	All	100	—	ns typ	OUT 1 Load = 100 Ω, C_{EXT} = 13 pF. Digital Inputs = 0 V to V_{DD} or V_{DD} to 0 V.
DIGITAL TO ANALOG GLITCH IMPULSE	All	1000	—	nV-sec typ	V_{REF} = 0 V. All digital inputs 0 V to V_{DD} or V_{DD} to 0 V. Measured using Model 50K as output amplifie
MULTIPLYING FEEDTHROUGH ERROR[3] (V_{REF} to OUT1)	All	1.0	—	mV p-p typ	V_{REF} = ±10 V, 10 kHz sine wave.
OUTPUT CURRENT SETTLING TIME	All	0.6	—	μs typ	To 0.01% of full-scale range. OUT 1 Load = 100 Ω, C_{EXT} = 13 pF. Digital Inputs = 0 V to V_{DD} or V_{DD} to 0 V.
OUTPUT CAPACITANCE					
C_{OUT1} (Pin 1)	All	200	200	pF max	Digital Inputs
C_{OUT2} (Pin 2)	All	70	70	pF max	= V_{IH}
C_{OUT1} (Pin 1)	All	70	70	pF max	Digital Inputs
C_{OUT2} (Pin 2)	All	200	200	pF max	= V_{IL}

NOTES
[1]Temperature range as follows: J, K versions, 0°C to +70°C; A, B versions, −25°C to +85°C; S, T versions, −55°C to +125°C.
[2]Guaranteed by design but not production tested.
[3]To minimize feedthrough in the ceramic package (Suffix D) the user must ground the metal lid.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to GND	+17 V
V_{REF} to GND	±25 V
V_{RFB} to GND	±25 V
Digital Input Voltage to GND	–0.3 V, V_{DD} + 0.3 V
OUT 1, OUT 2 to GND	–0.3 V, V_{DD} + 0.3 V
Power Dissipation (Any Package)	
To +75°C	450 mW
Derates above +75°C	6 mW/°C
Operating Temperature Range	
Commercial (J, K Versions)	0°C to +70°C
Industrial (A, B Versions)	–25°C to +85°C
Extended (S, T Versions)	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 10 secs)	+300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7541A features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TERMINOLOGY

RELATIVE ACCURACY

Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is expressed in % of full-scale range or (sub)multiples of 1 LSB.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is the difference between the *measured* change and the *ideal* 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB max over the operating temperature range insures monotonicity.

GAIN ERROR

Gain error is a measure of the output error between an ideal DAC and the actual device output. For the AD7541A, ideal maximum output is

$$-\left(\frac{4095}{4096}\right)(V_{REF}).$$

Gain error is adjustable to zero using external trims as shown in Figures 4, 5 and 6.

OUTPUT LEAKAGE CURRENT

Current which appears at OUT1 with the DAC loaded to all 0s or at OUT2 with the DAC loaded to all 1s.

MULTIPLYING FEEDTHROUGH ERROR

AC error due to capacitive feedthrough from V_{REF} terminal to OUT1 with DAC loaded to all 0s.

OUTPUT CURRENT SETTLING TIME

Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to full scale.

PROPAGATION DELAY

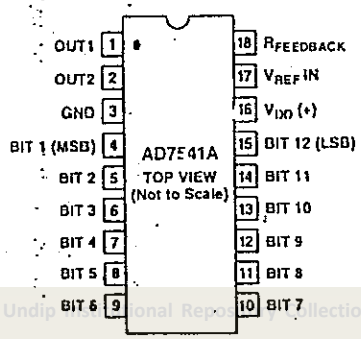
This is a measure of the internal delay of the circuit and is measured from the time a digital input changes to the point at which the analog output at OUT1 reaches 90% of its final value.

DIGITAL-TO-ANALOG CHARGE INJECTION (QDA)

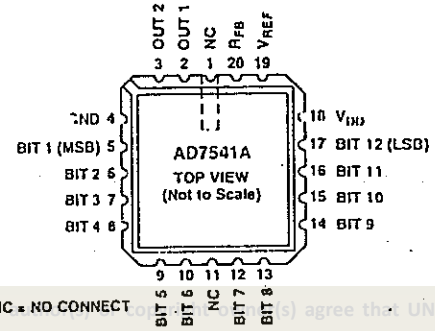
This is a measure of the amount of charge injected from the digital inputs to the analog outputs when the inputs change state. It is usually specified as the area of the glitch in nV secs and is measured with V_{REF} = GND and a Model 50K as the output op amp, C1 (phase compensation) = 0 pF.

PIN CONFIGURATIONS

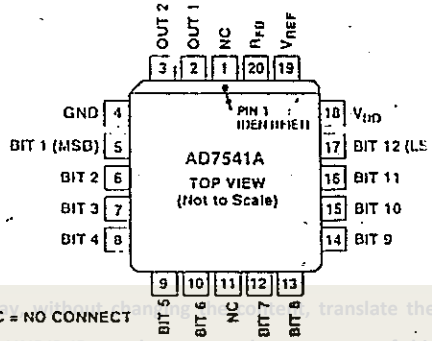
DIP/SOIC



LCCC



PLCC



AD7541A

GENERAL CIRCUIT INFORMATION

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used—that is, the binarily weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

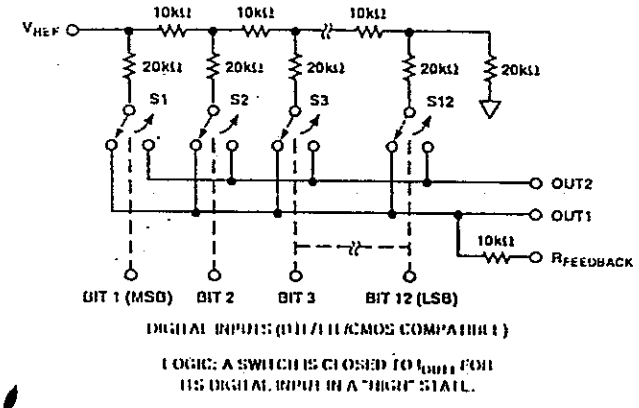


Figure 1. Functional Diagram (Inputs HIGH)

The input resistance at V_{REF} (Figure 1) is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristic resistance and is equal to value "R"). Since R_{IN} at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. (If a current source is used, a low temperature coefficient external R_{FB} is recommended to define scale factor.)

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs LOW and all digital inputs HIGH are shown in Figures 2 and 3. In Figure 2 with all digital inputs LOW, the reference current is switched to OUT2. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate, while the I_{4096} current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The ON capacitance of the output N-channel switch is 200 pF, as shown on the OUT2 terminal. The OFF switch capacitance is 70 pF, as shown on the OUT1 terminal. Analysis of the circuit for all digital inputs HIGH, as shown in Figure 3 is similar to Figure 2; however, the ON switches are now on terminal OUT1, hence the 200 pF at that terminal.

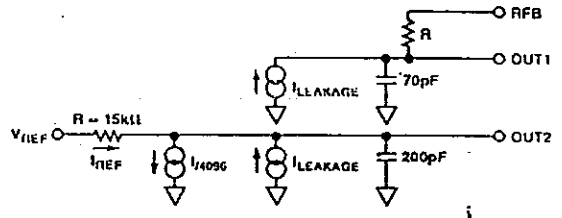


Figure 2. DAC Equivalent Circuit All Digital Inputs LOW

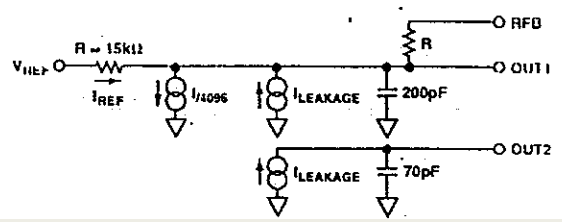


Figure 3. DAC Equivalent Circuit All Digital Inputs HIGH

APPLICATIONS

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 4 shows the analog circuit connections required for unipolar binary (2-quadrant multiplication) operation. With a dc reference voltage or current (positive or negative polarity) applied at Pin 17, the circuit is a unipolar D/A converter. With an ac reference voltage or current, the circuit provides 2-quadrant multiplication (digitally controlled attenuation). The input/output relationship is shown in Table II.

R1 provides full-scale trim capability [i.e., load the DAC register to 1111 1111 1111, adjust R1 for $V_{OUT} = -V_{REF}$ (4095/4096)]. Alternatively, Full Scale can be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude.

C1 phase compensation (10 pF to 25 pF) may be required for stability when using high speed amplifiers. (C1 is used to cancel the pole formed by the DAC internal feedback resistance and output capacitance at OUT1).

Amplifier A1 should be selected or trimmed to provide $V_{OS} \leq$ 10% of the voltage resolution at V_{OUT}. Additionally, the amplifier should exhibit a bias current which is low over the temperature range of interest (bias current causes output offset at V_{OUT} equal to I_B times the DAC feedback resistance, nominally 11 kΩ). The AD544L is a high speed implanted FET input op amp with low factory-trimmed V_{OS}.

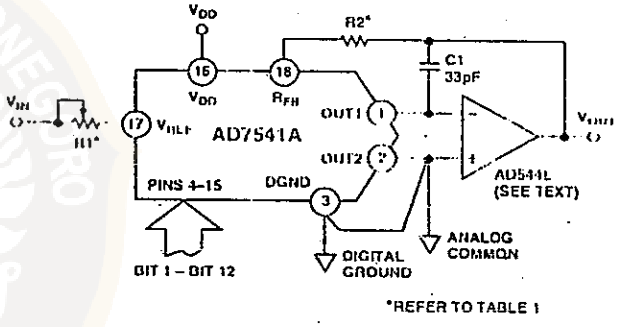


Figure 4. Unipolar Binary Operation

Table I. Recommended Trim Resistor Values vs. Grades

Trim Resistor	JN/AQ/SD	KN/BQ/TD
R1	100 Ω	100 Ω
R2	47 Ω	33 Ω

Table II. Unipolar Binary Code Table for Circuit of Figure 4

Binary Number in DAC MSB		LSB	Analog Output, V_{OUT}
1111	1111	1111	$-V_{IN}\left(\frac{4095}{4096}\right)$
1000	0000	0000	$-V_{IN}\left(\frac{2048}{4096}\right) = -1/2\ V_{IN}$
0000	0000	0001	$-V_{IN}\left(\frac{1}{4096}\right)$
0000	0000	0000	0 Volts

ANALOG DEVICES

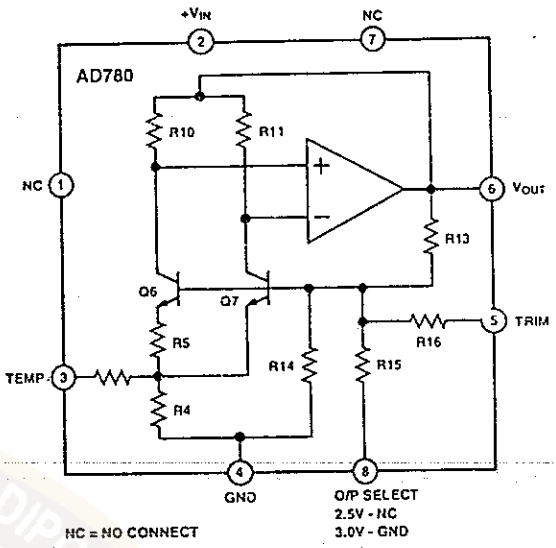
2.5 V/3.0 V High Precision Reference

AD780

FEATURES

Pin-Programmable 2.5 V or 3.0 V Output
Ultralow Drift: 3 ppm/°C max
High Accuracy: 2.5 V or 3.0 V ± 1 mV max
Low Noise: 100 nV/√Hz
Noise Reduction Capability
Low Quiescent Current: 1 mA max
Output Trim Capability
Plug-In Upgrade for Present References
Temperature Output Pin
Series or Shunt Mode Operation (±2.5 V, ±3.0 V)

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD780 is an ultrahigh precision bandgap reference voltage which provides a 2.5 V or 3.0 V output from inputs between 4.0 V and 36 V. Low initial error and temperature drift combined with low output noise and the ability to drive any value of capacitance make the AD780 the ideal choice for enhancing the performance of high resolution ADCs and DACs and for any general purpose precision reference application. A unique low headroom design facilitates a 3.0 V output from a 5.0 V ± 10% input, providing a 20% boost to the dynamic range of an ADC, over performance with existing 2.5 V references.

The AD780 can be used to source or sink up to 10 mA and can be used in series or shunt mode, thus allowing positive or negative output voltages without external components. This makes it suitable for virtually any high performance reference application. Unlike some competing references, the AD780 has no "region of possible instability." The part is stable under all load conditions when a 1 µF bypass capacitor is used on the supply.

A temperature output pin is provided on the AD780. This provides an output voltage that varies linearly with temperature, allowing the AD780 to be configured as a temperature transducer while providing a stable 2.5 V or 3.0 V output.

The AD780 is a pin-compatible performance upgrade for the LT1019(A)–2.5 and the AD680. The latter is targeted toward low power applications.

The AD780 is available in two grades in plastic DIP, SOIC and cerdip packages. The AD780AN, AD780AR, AD780BN and AD780BR are specified for operation from –40°C to +85°C. The AD780SQ and AD780SQ/883B are specified for –55°C to +125°C operation.

PRODUCT HIGHLIGHTS

1. The AD780 provides a pin-programmable 2.5 V or 3.0 V output from a 4 V to 36 V input.
2. Laser trimming of both initial accuracy and temperature coefficients results in low errors over temperature without the use of external components. The AD780BN has a maximum variation of 0.8 mV from –40°C to +85°C.
3. For applications requiring even higher accuracy, an optional fine-trim connection is provided.
4. The AD780 noise is extremely low, typically 4 µV p-p from 0.1 Hz to 10 Hz and a wideband spectral noise density of typically 100 nV/√Hz. This can be further reduced if desired, by simply using two external capacitors.
5. The temperature output pin enables the AD780 to be configured as a temperature transducer while providing a stable output reference voltage.

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703

AD780—SPECIFICATIONS (T_A = +25°C, V_{IN} = +5 V unless otherwise noted)

Parameter	AD780AN/AR/SQ Min	Typ	Max	AD780BN/BR Min	Typ	Max	Units
OUTPUT VOLTAGE							
2.5 V Out	2.495		2.505	2.499		2.501	Volts
3.0 V Out	2.995		3.005	2.999		3.001	Volts
OUTPUT VOLTAGE DRIFT[1]							
–40°C to +85°C			7			3	ppm/°C
–55°C to +125°C			20				ppm/°C
LINE REGULATION							
2.5 V Output, 4 V ≤ $+V_{IN}$ ≤ 36 V							
T_{MIN} to T_{MAX}			10			*	µV/V
3.0 V Output, 4.5 V ≤ $+V_{IN}$ ≤ 36 V							
T_{MIN} to T_{MAX}			10			*	µV/V
LOAD REGULATION, SERIES MODE							
Sourcing 0 < I_{OUT} < 10 mA			50			*	µV/mA
T_{MIN} to T_{MAX}			75			*	µV/mA
Sinking –10 < I_{OUT} < 0 mA			75			*	µV/mA
–40°C to +85°C			75			*	µV/mA
–55°C to +125°C			150			*	µV/mA
LOAD REGULATION, SHUNT MODE							
I < I_{SHUNT} < 10 mA			75			*	µV/mA
QUIESCENT CURRENT, 2.5 V SERIES MODE[2]							
–40°C to +85°C		0.75	1.0		*	*	mA
–55°C to +125°C		0.8	1.3		*	*	mA
MINIMUM SHUNT CURRENT		0.7	1.0		*	*	mA
OUTPUT NOISE							
0.1 Hz to 10 Hz		4			*	*	µV p-p
Spectral Density, 100 Hz		100			*	*	nV/√Hz
LONG TERM STABILITY[3]		20			*		±ppm/1000 Hr
TRIM RANGE	4.0			*			±%
TEMPERATURE PIN							
Voltage Output @ 25°C	500	560	620	*	*	*	mV
Temperature Sensitivity		1.9			*		mV/°C
Output Resistance		3			*		kΩ
SHORT CIRCUIT CURRENT TO GROUND		30			*		mA
TEMPERATURE RANGE							
Specified Performance (A, B)	–40		+85	*		*	°C
Operating Performance (A, B)[4]	–55		+125	*		*	°C
Specified Performance (S)	–55		+125	*		*	°C
Operating Performance (S)	–55		+125	*		*	°C

NOTES

[1]Maximum output voltage drift is guaranteed for all packages.

[2]3.0 V mode typically adds 100 µA to the quiescent current. Also, Iq increases by 2 µA/V above an input voltage of 5 V.

[3]The long term stability specification is noncumulative. The drift in subsequent 1000 hr. periods is significantly lower than in the first 1000 hr. period.

[4]The operating temperature range is defined as the temperature extremes at which the device will still function. Parts may deviate from their specified performance outside their specified temperature range.

*Same as AD780AN/AR/SQ specification.

Specifications subject to change without notice.

CAUTION

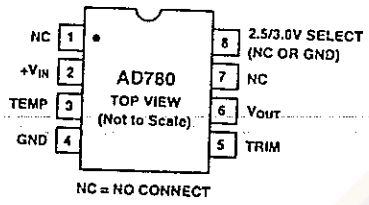
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD780 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ABSOLUTE MAXIMUM RATINGS*

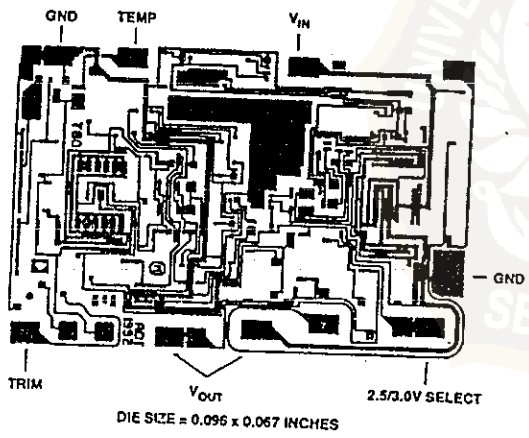
V_{IN} to Ground ..... 36 V
Trim Pin to Ground ..... 36 V
Temp Pin to Ground ..... 36 V
Power Dissipation (25°C) ..... 500 mW
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C
Output Protection: Output safe for indefinite short to ground and momentary short to V_{IN}.
ESD Classification ..... Class 1 (1000 V)

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions above those indicated in the operational specification is not implied. Exposure to absolute maximum specifications for extended periods may affect device reliability.

PIN CONFIGURATION
8-Pin Plastic DIP, SOIC and Cerdip Packages



DIE LAYOUT



NOTES
Both V_{OUT} pads should be connected to the output
Die Thickness: The standard thickness of Analog Devices Bipolar dice is 24 mils ±2 mils.
Die Dimensions: The dimensions given have a tolerance of ±2 mils.
Backing: The standard backside surface is silicon (not plated). Analog Devices does not recommend gold-backed dice for most applications.
Edges: A diamond saw is used to separate wafers into dice thus providing perpendicular edges half-way through the die.

In contrast to scribed dice, this technique provides a more uniform die shape and size. The perpendicular edges facilitate handling (such as tweezer pick-up) while the uniform shape and size simplifies substrate design and die attach.
Top Surface: The standard top surface of the die is covered by a layer of glassivation. All areas are covered except bonding pads and scribe lines.
Surface Metalization: The metalization to Analog Devices bipolar dice is aluminum. Minimum thickness is 10,000Å.
Bonding Pads: All bonding pads have a minimum size of 4.0 mils by 6.0 mils. The passivation windows have a 3.6 mils by 5.6 mils minimum size.

ORDERING GUIDE

Model	Initial Error	Temperature Coefficient	Temperature Range	Package
AD780AN	5 mV	7 ppm/°C	–40°C to +85°C	Plastic
AD780AR	5 mV	7 ppm/°C	–40°C to +85°C	SOIC
AD780BN	1 mV	3 ppm/°C	–40°C to +85°C	Plastic
AD780BR	1 mV	3 ppm/°C	–40°C to +85°C	SOIC
AD780SQ	5 mV	20 ppm/°C	–55°C to +125°C	Cerdip
AD780SQ/883B	5 mV	20 ppm/°C	–55°C to +125°C	Cerdip

THEORY OF OPERATION

Bandgap references are the high performance solution for low supply voltage and low power voltage reference applications. In this technique a voltage with a positive temperature coefficient is combined with the negative coefficient of a transistor's Vbe to produce a constant *bandgap* voltage.

In the AD780, the bandgap cell contains two npn transistors (Q6 and Q7) which differ in emitter area by 12×. The difference in their Vbe's produces a PTAT current in R5. This in turn produces a PTAT voltage across R4, which when combined with the Vbe of Q7, produces a voltage Vbg that does not vary with temperature. Precision laser trimming of the resistors and other patented circuit techniques are used to further enhance the drift performance.

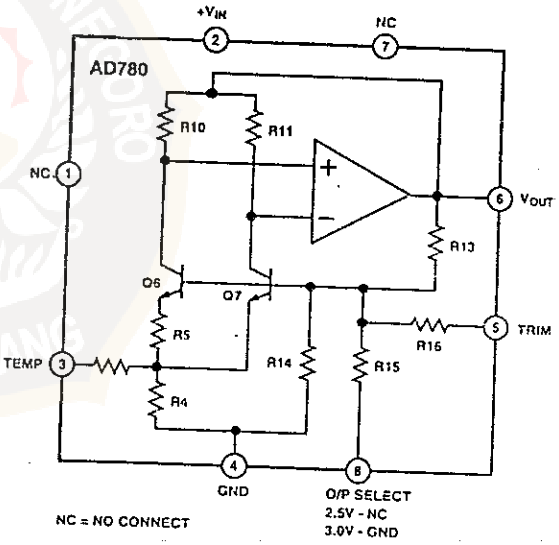


Figure 1. Schematic Diagram

The output voltage of the AD780 is determined by the configuration of resistors R13, R14 and R15 in the amplifier's feedback loop. This sets the output to either 2.5 V or 3.0 V depending on whether R15 (Pin 8) is grounded or not connected.

A unique feature of the AD780 is the low headroom design of the high gain amplifier which produces a precision 3 V output from an input voltage as low as 4.5 V (or 2.5 V from a 4.0 V input). The amplifier design also allows the part to work with $V_{IN} = V_{OUT}$ when current is forced into the output terminal. This allows the AD780 to work as a two terminal shunt regulator providing a –2.5 V or - 3.0 V reference voltage output without external components.

The PTAT voltage is also used to provide the user with a thermometer output voltage (at Pin 3) which increases at a rate of approximately 2 mV/°C.

The AD780's NC Pin 7 is a 20 kΩ resistor to V+ which is used solely for production test purposes. Users who are currently using the LT1019 self-heater pin (Pin 7) must take into account the different load on the heater supply.

APPLYING THE AD780

The AD780 can be used without any external components to achieve specified performance. If power is supplied to Pin 2 and Pin 4 is grounded, Pin 6 provides a 2.5 V or 3.0 V output depending on whether Pin 8 is left unconnected or grounded.

A bypass capacitor of 1 µF (V_{IN} to GND) should be used if the load capacitance in the application is expected to be greater than 1 nF. The AD780 in 2.5 V mode typically draws 700 µA of Iq at 5 V. This increases by ~2 µA/V up to 36 V.

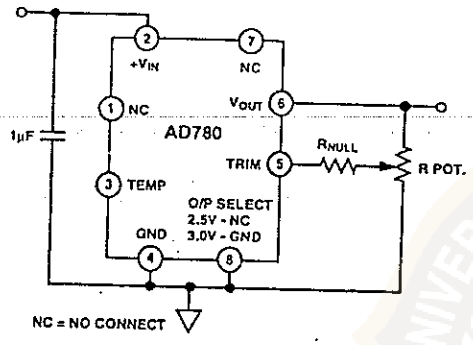


Figure 2. Optional Fine Trim Circuit

Initial error can be nulled using a single 25 kΩ potentiometer connected between V_{OUT}, Trim and GND. This is a coarse trim with an adjustment range of ±4% and is only included here for compatibility purposes with other references. A fine trim can be implemented by inserting a large value resistor (e.g. 1–5 MΩ) in series with the wiper of the potentiometer. See Figure 2 above. The trim range, expressed as a fraction of the output, is simply greater than or equal to 2.1 kΩ/R_{NULL} for either the 2.5 V or 3.0 V mode.

The external null resistor affects the overall temperature coefficient by a factor equal to the percentage of V_{OUT} nulled.

For example a 1 mV (.03%) shift in the output caused by the trim circuit, with a 100 ppm/°C null resistor will add less than 0.06 ppm/°C to the output drift (0.03% × 200 ppm/°C, since the resistors internal to the AD780 also have temperature coefficients of less than 100 ppm/°C).

NOISE PERFORMANCE

The impressive noise performance of the AD780 can be further improved if desired by the addition of two capacitors: a load capacitor C1 between the output and ground, and a compensation capacitor C2 between the TEMP pin and ground. Suitable values are shown in Figure 3.

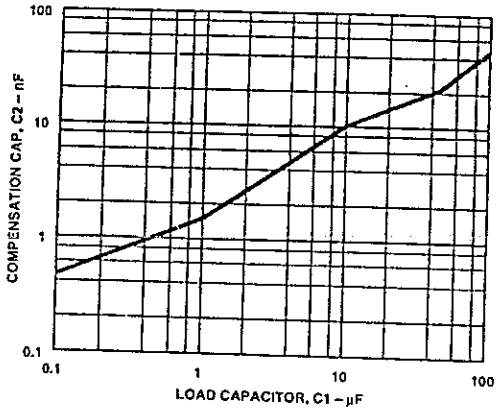


Figure 3. Compensation and Load Capacitor Combinations

C1 and C2 also improve the settling performance of the AD780 when subjected to load transients. The improvement in noise performance is shown in Figures 4, 5 and 6 following.

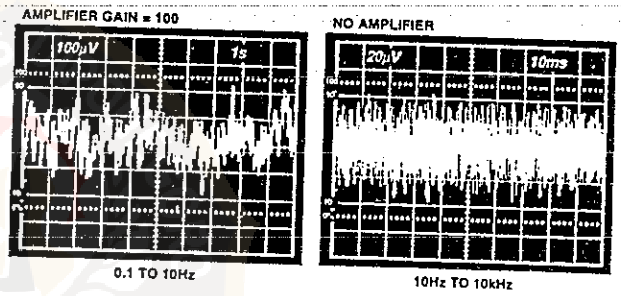


Figure 4. Stand-Alone Noise Performance

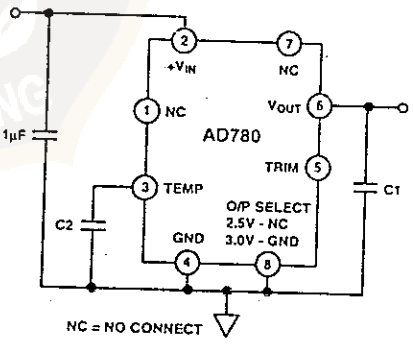


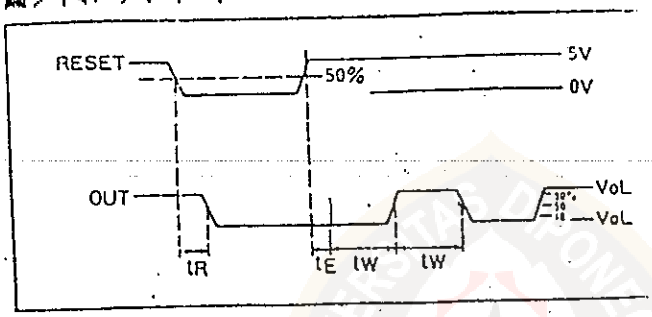
Figure 5. Noise Reduction Circuit

Lampiran C.4. Data Karakteristik 8640N

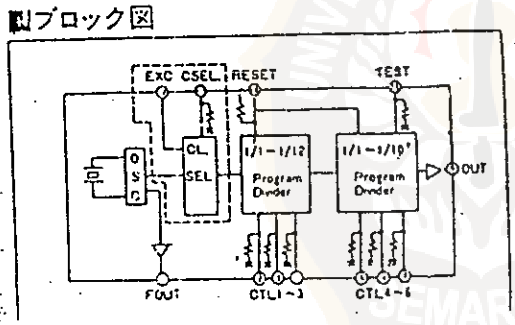
(PROGRAMMABLE CLOCK PULSE GENERATOR)

SPG-8640N

■タイミングチャート



■ブロック図



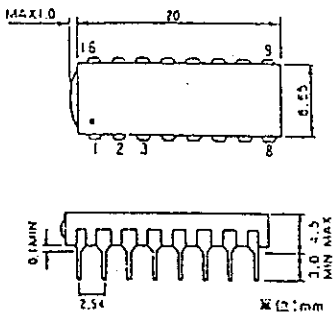
■PIN CONNECTIONS

1. NC	16. V_{DD}
2. CTL3	15. NC
3. CTL2	14. RESET
4. CTL1	13. NC(CSEL)
5. CTL6	12. NC(EXC)
6. CTL5	11. FOUT
7. CTL4	10. TEST
8. Vss	9. OUT

NC:外部接続はしないでください。

■8640BN

設定端子		CTL4	0	0	0	0	1	1	1	1
		CTL5	0	0	1	1	0	0	1	1
CTL1	CTL2	CTL6	0	1	0	1	0	1	0	1
0	0	0	1M	100 K	10 K	1K	100	10	1	1/10
0	0	1	100K	10 K	1 K	100	10	1	1/10	1/100
0	1	0	50OK	50 K	5 K	500	50	5	1/ 2	1/20
0	1	1	333.3K*1	33.3K	3.3K	333.3	33.3	3.33	1/ 3	1/30
1	0	0	250K	25 K	2.5K	250	25	2.5	1/ 4	1/40
1	0	1	200K*2	20 K	2 K	200	20	2	1/ 5	1/50
1	1	0	166.6K	16.6K	1.6K	166.6	16.6	1.6	1/ 6	1/60
1	1	1	83.3K	8.3K	833.3	83.3	8.3	0.83	1/12	1/120



電気的特性

Temp.=25℃ V_{DD}=5V

	項目	MIN	TYP	MAX	UNITS	
V_{DD}	動作電圧	4.5	5	5.5	V	
V_{IL}	入力電圧 論理値：0	0.0		0.8	V	
V_{IH}	入力電圧 論理値：1	4		V_{DD}	V	
I_{IH1}	入力電流 REST 論理値：1			0.5	μA	
I_{IL1}	入力電流 REST 論理値：0	−5		−30	μA	
I_{IH2}	入力電流 CTL,TEST,CSELEXO 論理値：	5		30	μA	( )は 8640Nのみ
I_{IL2}	入力電流 CTL,TEST,CSELEXO 論理値：0	−0.5			μA	( )は 8640Nのみ
I_{OL}	最大出力電流			5	mA	
V_{OH}	出力電圧 論理値：1	4		V_{DD}	V	−40μA
V_{OL}	出力電圧 論理値：0	0.0		0.4	V	1.6mA
t_R	リセット遅延時間			1.0	μsec	CL=15pF
t_A	リセット発振周期誤差			未	μsec	CL=15pF
	水晶信号[illegible]					8640Nのみ

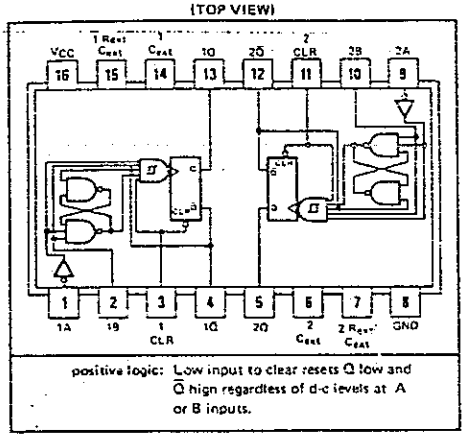
Lampiran C.5. Data Karakteristik 74221

TYPES SN54221, SN54LS221, SN74221, SN74LS221
DUAL MONOSTABLE MULTIVIBRATORS
WITH SCHMITT-TRIGGER INPUTS

- SN54221, SN54LS221, SN74221 and SN74LS221 Are Dual Versions of Highly Stable SN54121, SN74121 One-Shots on a Monolithic Chip
- SN54221 and SN74221 Demonstrate Electrical and Switching Characteristics That Are Virtually Identical to the SN54121, SN74121 One-Shots
- Pin-Out Is Identical to the SN54123 SN74123, SN54LS123, SN74LS123
- Overriding Clear Terminates Output Pulse

TYPE	TYPICAL POWER DISSIPATION	MAXIMUM OUTPUT PULSE LENGTH
SN54221	130 mW	21 s
SN74221	130 mW	29 s
SN54LS221	23 mW	49 s
SN74LS221	23 mW	70 s

SN54221, SN54LS221 . . . J OR W PACKAGE
SN74221, SN74LS221 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: Low input to clear resets Q low and $\overline{Q}$ high regardless of d-c levels at A or B inputs.

description

The '221 and 'LS221 are monolithic dual multivibrators with performance characteristics virtually identical to those of the '121. Each multivibrator features a negative-transition-triggered input and a positive-transition-triggered input either of which can be used as an inhibit input.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions of the A and B inputs and are a function of the timing components, or the output pulses can be terminated by the overriding clear. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 35 nanoseconds to the maximums shown in the above table by choosing appropriate timing components. With R_{ext} = 2 kΩ and C_{ext} = 0, an output pulse of typically 30 nanoseconds is achieved which may be used as a d-c-triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length. Typical triggering and clearing sequences are illustrated as a part of the switching characteristics waveforms.

Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and V_{CC} ranges for more than six decades of timing capacitance (10 pF to 10 μF) and more than one decade of timing resistance (2 kΩ to 30 kΩ for the SN54221, 2 kΩ to 40 kΩ for the SN74221, 2 kΩ to 70 kΩ for the SN54LS221, and 2 kΩ to 100 kΩ for the SN74LS221). Throughout these ranges, pulse width is defined by the relationship: $t_{w(out)} = C_{ext}R_{ext}\ ln2 \approx 0.7\ C_{ext}R_{ext}$. In circuits where pulse cutoff is not critical, timing capacitance up to 1000 μF and timing resistance as low as 1.4 kΩ may be used. Also, the range of jitter-free output pulse widths is extended if V_{CC} is held to 5 volts and free-air temperature is 25°C. Duty cycles as high as 90% are achieved when using maximum recommended R_T. Higher duty cycles are available if a certain amount of pulse-width jitter is allowed.

FUNCTION TABLE
(EACH MONOSTABLE)

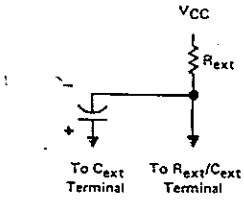
INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⊓	⊔
H	↓	H	⊓	⊔
↑	L	H	⊓	⊔

Also see description and switching characteristics

See explanation of function tables on page 3-8.

The variance in output pulse width from device to device is typically less than ±0.5% for given external timing components. An example of this distribution for the '221 is shown in Figure 2. Variations in output pulse width versus supply voltage and temperature for the '221 are shown in Figure 3 and 4, respectively.

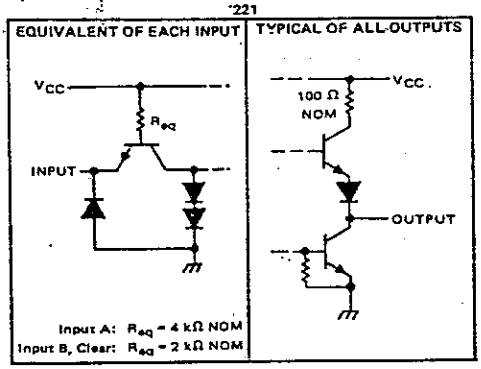
Pin assignments for these devices are identical to those of the SN54123/SN74123 or SN54LS123/SN74LS123 so that the '221 or 'LS221 can be substituted for those products in systems not using the retrigger by merely changing the value of R_{ext} and/or C_{ext}.



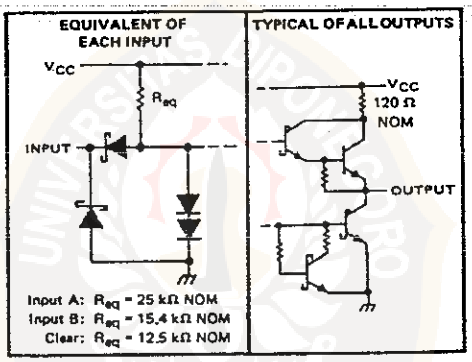
TIMING COMPONENT CONNECTIONS

schematics of inputs and outputs

'221



'LS221



recommended operating conditions

		SN54221			SN74221			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Rate of rise or fall of input pulse, dv/dt	Schmitt input, B	1			1			V/s
	Logic input, A	1			1			V/μs
Input pulse width	A or B, $t_{w(in)}$	50			50			ns
	Clear, $t_{w(clear)}$	20			20			
Clear-inactive-state setup time, t_{su}		15			15			ns
External timing resistance, R_{ext}		1.4		30	1.4		40	kΩ
External timing capacitance, C_{ext}		0		1000	0		1000	μF
Output duty cycle	R_{ext} = 2 kΩ			67			67	%
	R_{ext} = MAX R_{ext}			90			90	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{T+}	Positive-going threshold voltage at A input	V_{CC} = MIN			1.4	2	V
V_{T-}	Negative-going threshold voltage at A input	V_{CC} = MIN		0.8	1.4		V
V_{T+}	Positive-going threshold voltage at B input	V_{CC} = MIN			1.55	2	V
V_{T-}	Negative-going threshold voltage at B input	V_{CC} = MIN		0.8	1.35		V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = −800 μA		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V	Input A			40	μA
			Input B, Clear			80	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V	Input A			−1.6	mA
			Input B, Clear			−3.2	
I_{OS}	Short-circuit output current§	V_{CC} = MAX	SN54221	−20		−55	mA
			SN74221	−18		−55	
I_{CC}	Supply current	V_{CC} = MAX	Quiescent		26	50	mA
			Triggered		46	80	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A	Q	C_L = 15 pF, R_L = 400 Ω, See Figure 1 and Note 2	C_{ext} = 80 pF, R_{ext} = 2 kΩ		45	70	ns
	B	Q				35	55	
t_{PHL}	A	$\overline{Q}$				50	80	ns
	B	$\overline{Q}$				40	65	
t_{PHL}	Clear	Q					27	ns
t_{PLH}	Clear	$\overline{Q}$					40	ns
$t_{w(out)}$	A or B	Q or $\overline{Q}$		C_{ext} = 80 pF, R_{ext} = 2 kΩ	70	110	150	ns
				C_{ext} = 0, R_{ext} = 2 kΩ	20	30	50	
				C_{ext} = 100 pF, R_{ext} = 10 kΩ	650	700	750	
				C_{ext} = 1 μF, R_{ext} = 10 kΩ	6.5	7	7.5	ms

¶t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
$t_{w(out)}$ ≡ Output pulse width
NOTE 2: Load circuit is shown on page 3-10.

recommended operating conditions

		SN54LS221			SN74LS221			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Rate of rise or fall of input pulse, dv/dt	Schmitt, B	1			1			V/s
	Logic input, A	1			1			V/μs
Input pulse width	A or B, $t_{w(in)}$	50			50			ns
	Clear, $t_{w(clear)}$	40			40			
Clear-inactive-state setup time, t_{su}		15			15			ns
External timing resistance, R_{ext}		1.4		70	1.4		100	kΩ
External timing capacitance, C_{ext}		0		1000	0		1000	μF
Output duty cycle	R_T = 2 kΩ			50			50	%
	R_T = MAX R_{ext}			90			90	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS221			SN74LS221			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{T+}	Positive-going threshold voltage at A input		V_{CC} = MIN			1.0	2		1.0	2	V
V_{T-}	Negative-going threshold voltage at A input		V_{CC} = MIN		0.7	1.0		0.8	1.0		V
V_{T+}	Positive-going threshold voltage at B input		V_{CC} = MIN			1.0	2		1.0	2	V
V_{T-}	Negative-going threshold voltage at B input		V_{CC} = MIN		0.7	0.9		0.8	0.9		V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	Input A	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
		Input B					−0.8			−0.8	
		Clear					−0.8			−0.8	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX	Quiescent		4.7	11		4.7	11	mA
				Triggered		19	27		19	27	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

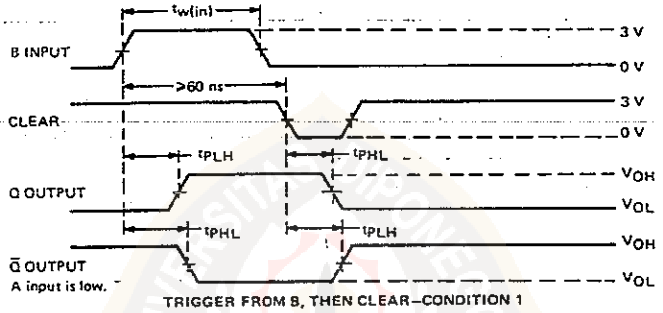
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A	Q	C_L = 15 pF, R_L = 2 kΩ, See Figure 1 and Note 3	C_{ext} = 80 pF R_{ext} = 2 kΩ		45	70	ns
	B	Q				35	55	
t_{PHL}	A	$\overline{Q}$				50	80	ns
	B	$\overline{Q}$				40	65	
t_{PHL}	Clear	Q				35	55	ns
t_{PLH}	Clear	$\overline{Q}$				44	65	ns
$t_{w(out)}$	A or B	Q or $\overline{Q}$		C_{ext} = 80 pF, R_{ext} = 2 kΩ	70	120	150	ns
				C_{ext} = 0, R_{ext} = 2 kΩ	20	47	70	
				C_{ext} = 100 pF, R_{ext} = 10 kΩ	600	670	750	
				C_{ext} = 1 μF, R_{ext} = 10 kΩ	6	6.7	7.5	ms

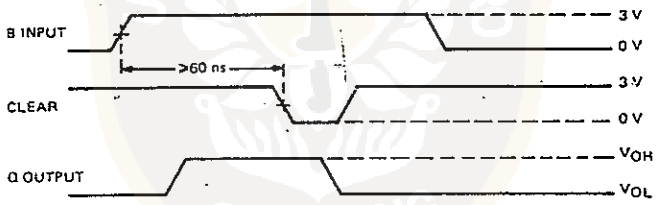
¶ t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
$t_{w(out)}$ ≡ Output pulse width

NOTE 3: Load circuit is shown on page 3-11.

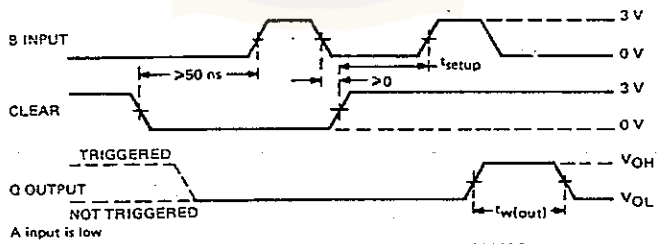
PARAMETER MEASUREMENT INFORMATION



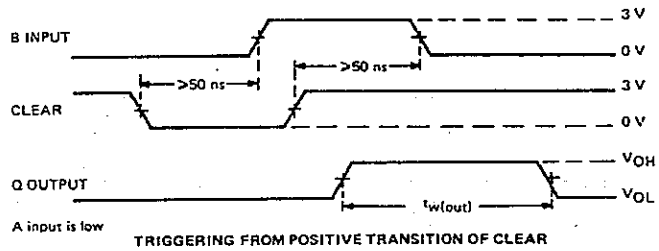
TRIGGER FROM B, THEN CLEAR—CONDITION 1



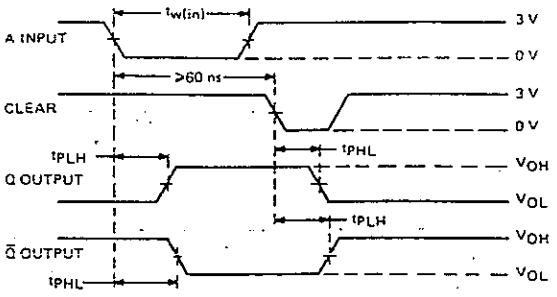
TRIGGER FROM B, THEN CLEAR—CONDITION 2



CLEAR OVERRIDING B, THEN TRIGGER FROM B

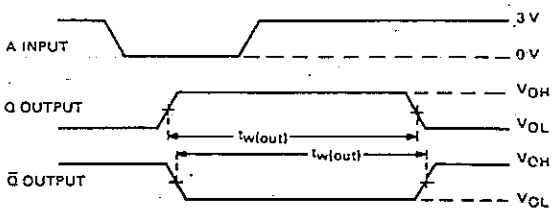


TRIGGERING FROM POSITIVE TRANSITION OF CLEAR



B input is high

TRIGGER FROM A, THEN CLEAR



B and clear inputs are high

TRIGGER FROM A

NOTES: A. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{out} ≈ 50 Ω; for '221, t_r ≤ 7 ns, t_f ≤ 7 ns, for 'LS221, t_r ≤ 15 ns, t_f ≤ 6 ns.
B. All measurements are made between the 1.5 V points of the indicated transitions for the '221 or between the 1.3 V points for the 'LS221.

TYPICAL CHARACTERISTICS ('221 ONLY)†

DISTRIBUTION OF UNITS
for
OUTPUT PULSE WIDTH

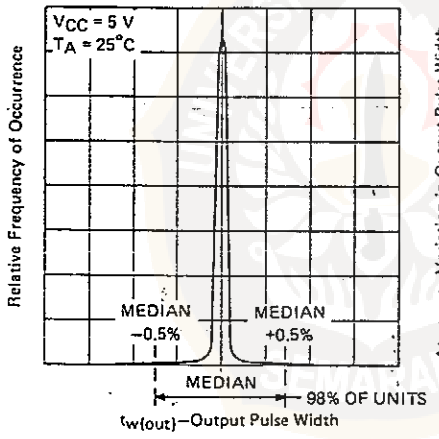


FIGURE 2

VARIATION IN OUTPUT PULSE WIDTH
vs
SUPPLY VOLTAGE

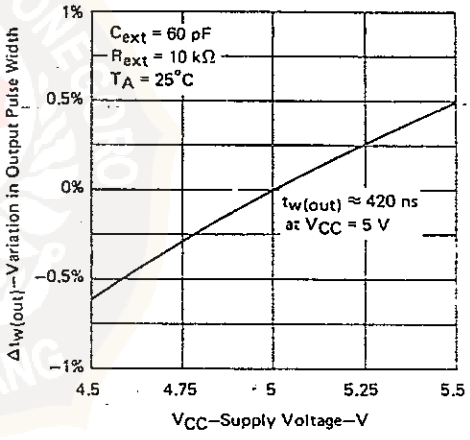


FIGURE 3

VARIATION IN OUTPUT PULSE WIDTH
vs
FREE-AIR TEMPERATURE

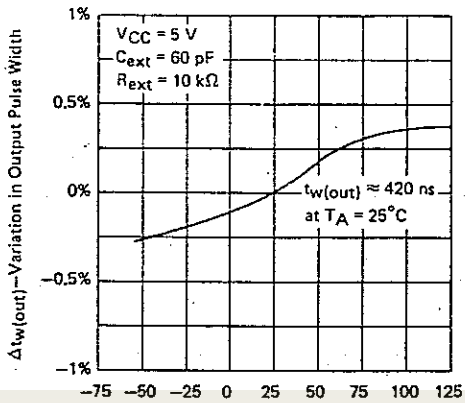


FIGURE 4

OUTPUT PULSE WIDTH
vs
TIMING RESISTOR VALUE

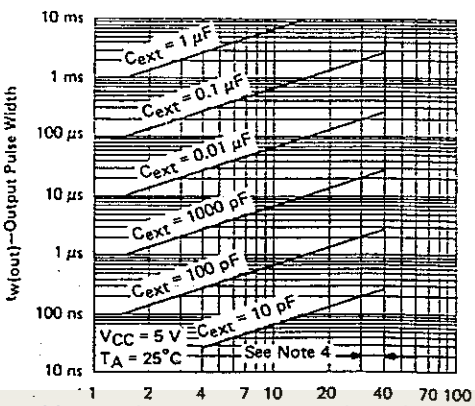


FIGURE 5

NOTE 4: These values of resistance exceed the maximum recommended for use over the full temperature range of the SN54221.

†Data for temperatures below 0°C and above 70°C, and for supply voltages below 4.75 V and above 5.25 V are applicable for the SN54221 only.

Lampiran C.6. Data Karakteristik 74193

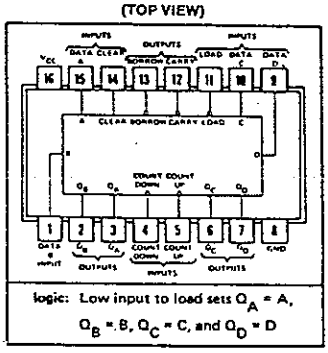
SN74192, SN74193, SN74LS192, SN74LS193
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

BULLETIN NO. DL-S 7611828, DECEMBER 1972– REVISED OCTOBER 1976

- Cascading Circuitry Provided Internally
- Synchronous Operation
- Individual Preset to Each Flip-Flop
- Fully Independent Clear Input

TYPES	TYPICAL MAXIMUM COUNT FREQUENCY	TYPICAL POWER DISSIPATION
'192, '193	32 MHz	325 mW
'LS192, 'LS193	32 MHz	95 mW

SN54', SN54LS'...J OR W PACKAGE
SN74', SN74LS'...J OR N PACKAGE
(TOP VIEW)



logic: Low input to load sets Q_A = A, Q_B = B, Q_C = C, and Q_D = D

description

These monolithic circuits are synchronous reversible (up/down) counters having a complexity of 55 equivalent gates. The '192, and 'LS192 circuits are BCD counters and the '193 and 'LS193 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.

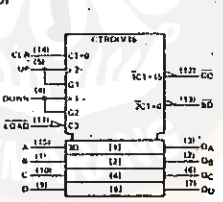
The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

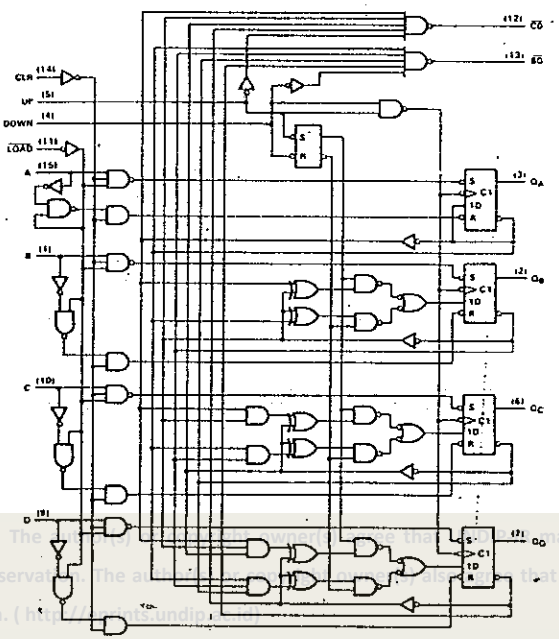
A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements. This reduces the number of clock drivers, etc., required for long words.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up- and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-up input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

'193, 'LS193 logic symbol



'193, 'LS193 logic diagrams (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN54'	SN54LS'	SN74'	SN74LS'	UNIT
Supply voltage, V_{CC} (see Note 1)	7	7	7	7	V
Input voltage	5.5	7	5.5	7	V
Operating free-air temperature range	−55 to 125		0 to 70		°C
Storage temperature range	−65 to 150		−65 to 150		°C

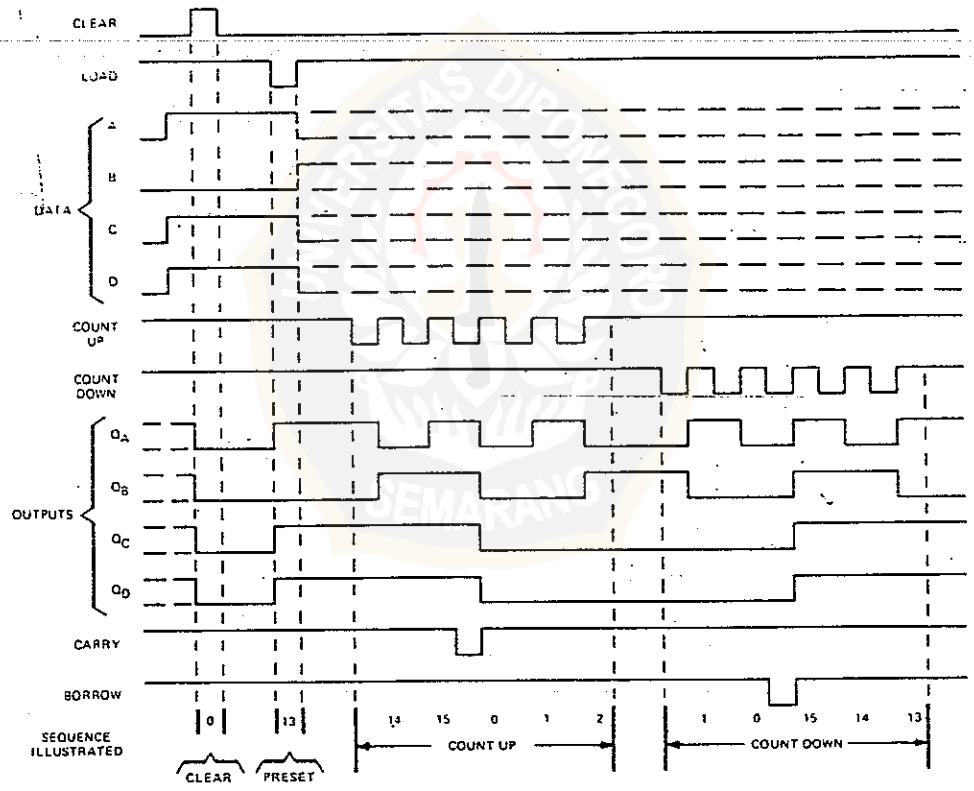
NOTE 1: Voltage values are with respect to network ground terminal.

'193, 'LS193 BINARY COUNTERS

typical clear, load, and count sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



NOTES: A. Clear overrides load, data, and count inputs.

B. When counting up, count-down input must be high; when counting down, count-up input must be high.

Lampiran C.7. Data Karakteristik 74175

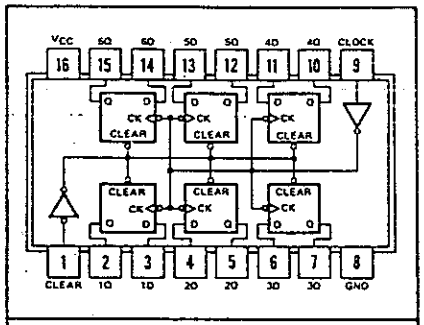
TYPES SN54174, SN54175, SN54LS174, SN54LS175, SN54S174, SN54S175, SN74174, SN74175, SN74LS174, SN74LS175, SN74S174, SN74S175
HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

BULLETIN NO. DL-S 7611803, DECEMBER 1972—REVISED OCTOBER 1976

'174, 'LS174, 'S174 . . . HEX D-TYPE FLIP-FLOPS
'175, 'LS175, 'S175 . . . QUADRUPLE D-TYPE FLIP-FLOPS

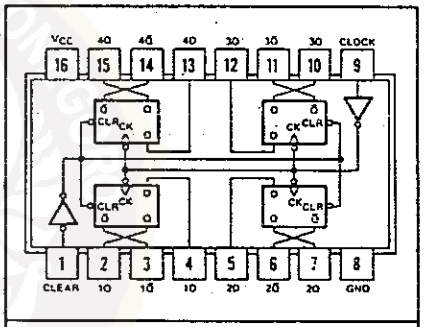
- '174, 'LS174, 'S174 Contain Six Flip-Flops with Single-Rail Outputs
- '175, 'LS175, 'S175 Contain Four Flip-Flops with Double-Rail Outputs
- Three Performance Ranges Offered: See Table Lower Right
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Applications include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators

SN54174, SN54LS174, SN54S174 . . . J OR W PACKAGE
SN74174, SN74LS174, SN74S174 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

SN54175, SN54LS175, SN54S175 . . . J OR W PACKAGE
SN74175, SN74LS175, SN74S175 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the '175, 'LS175, and 'S175 feature complementary outputs from each flip-flops.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These circuits are fully compatible for use with most TTL or DTL circuits.

FUNCTION TABLE
(EACH FLIP-FLOP)

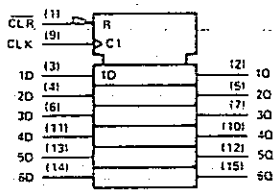
INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\bar{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established.
† = '175, 'LS175, and 'S175 only

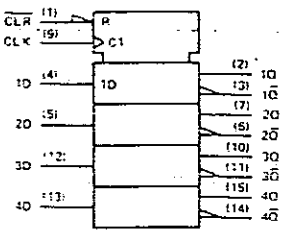
TYPES	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'174, '175	35 MHz	38 mW
'LS174, 'LS175	40 MHz	14 mW
'S174, 'S175	110 MHz	75 mW

logic symbols

'174, 'LS174, 'S174



'175, 'LS175, 'S175



TYPES SN54174, SN54175, SN74174, SN74175
HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54174, SN54175 Circuits . . . . . −55°C to 125°C
SN74174, SN74175 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54174, SN54175			SN74174, SN74175			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock or clear pulse, t_w		20			20			ns
Setup time, t_{su}	Data input	20			20			ns
	Clear inactive-state	25			25			ns
Data hold time, t_h		5			5			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	SN54'	−20		−57	mA
			SN74'	−18		−57	
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	'174		45	65	mA
			'175		30	45	

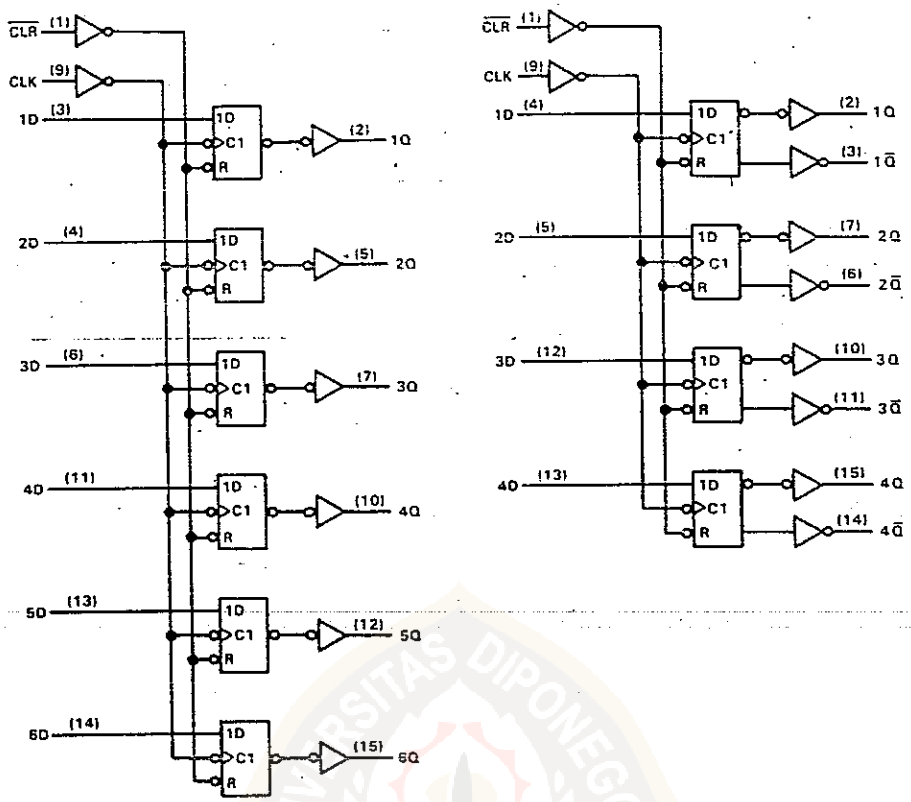
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω, See Note 3	25	35		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clear (SN54175, SN74175 only)			16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear			23	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			24	35	ns

NOTE 3: Load circuit and voltage waveforms are shown on page 3-10.

logic diagrams (positive logic)



Lampiran C.8. Data Karakteristik LM319

National Semiconductor

Voltage Comparators

LM119/LM219/LM319 High Speed Dual Comparator

General Description

The LM119 series are precision high speed dual comparators fabricated on a single monolithic chip. They are designed to operate over a wide range of supply voltages down to a single 5V logic supply and ground. Further, they have higher gain and lower input currents than devices like the LM710. The uncommitted collector of the output stage makes the LM119 compatible with RTL, DTL and TTL as well as capable of driving lamps and relays at currents up to 25 mA. Outstanding features include:

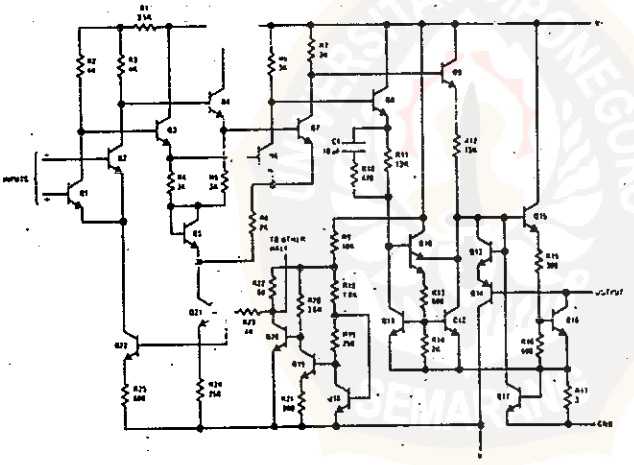
Features

- Two independent comparators
- Operates from a single 5V supply
- Typically 80 ns response time at ±15V
- Minimum fan-out of 2 each side
- Maximum input current of 1 μA over temperature
- Inputs and outputs can be isolated from system ground
- High common mode slew rate

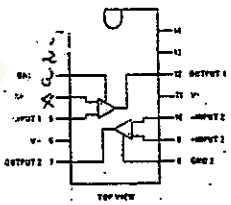
Although designed primarily for applications requiring operation from digital logic supplies, the LM119 series are fully specified for power supplies up to ±15V. It features faster response than the LM111 at the expense of higher power dissipation. However, the high speed, wide operating voltage range and low package count make the LM119 much more versatile than older devices like the LM711.

The LM119 is specified from −55°C to +125°C, the LM219 is specified from −25°C to +85°C, and the LM319 is specified from 0°C to +70°C.

Schematic and Connection Diagrams



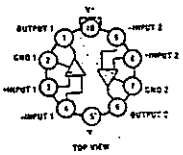
Dual-In-Line-Package



Order Number LM319N
See NS Package N14A

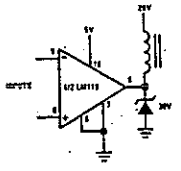
Order Number LM119J, LM219J or LM319J
See NS Package J14A

Metal Can Package

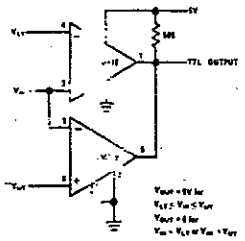


Order Number LM119H, LM219H or LM319H
See NS Package H10C

Typical Applications



Relay Driver



Window Detector

Absolute Maximum Ratings LM319

Total Supply Voltage	36V	Power Dissipation (Note 2)	500 mW
Output to Negative Supply Voltage	36V	Output Short Circuit Duration	10 sec
Ground to Negative Supply Voltage	25V	Operating Temperature Range LM319	0°C to 70°C
Ground to Positive Supply Voltage	18V	Storage Temperature Range	-65°C to 150°C
Differential Input Voltage	±5V	Lead Temperature (Soldering, 10 sec)	300°C
Input Voltage (Note 1)	±15V		

Electrical Characteristics (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 5k$		2.0	8.0	mV
Input Offset Current (Note 4)	$T_A = 25°C$		80	200	nA
Input Bias Current	$T_A = 25°C$		250	1000	nA
Voltage Gain	$T_A = 25°C$	8	40		V/mV
Response Time (Note 5)	$T_A = 25°C$ $V_S = \pm 15V$		80		ns
Saturation Voltage	$V_{IN} \leq -10$ mV, $I_{OUT} = 25$ mA $T_A = 25°C$		0.75	1.5	V
Output Leakage Current	$V_{IN} \geq 10$ mV, $V_{OUT} = 35V$, $V^- = V_{GND} = 0V$, $T_A = 25°C$		0.2	10	μA
Input Offset Voltage (Note 4)	$R_S \leq 5k$			10	mV
Input Offset Current (Note 4)				300	nA
Input Bias Current				1200	nA
Input Voltage Range	$V_S = \pm 15V$		±13		V
	$V^+ = 5V$, $V^- = 0$	1		3	V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -10$ mV, $I_{SINK} \leq 3.2$ mA		0.3	0.4	V
Differential Input Voltage				±5	V
Positive Supply Current	$T_A = 25°C$, $V^+ = 5V$, $V^- = 0$		4.3		mA
Positive Supply Current	$T_A = 25°C$ $V_S = \pm 15V$		8	12.5	mA
Negative Supply Current	$T_A = 25°C$ $V_S = \pm 15V$		3	5	mA

Note 1: For supply voltages less than ±15V the absolute maximum input voltage is equal to the supply voltage.

Note 2: The maximum junction temperature of the LM319 is 85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

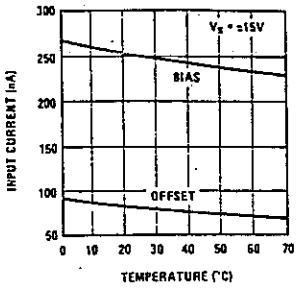
Note 3: These specifications apply for $V_S = \pm 15V$ and $0°C \leq T_A \leq 70°C$, unless otherwise stated. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

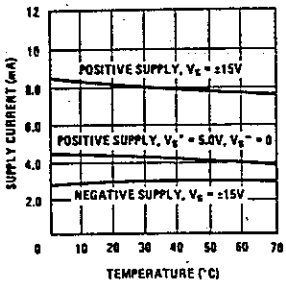
Note 5: The response time specified is for a 100 mV input step with 5 mV overdrive.

Typical Performance Characteristics - LM319

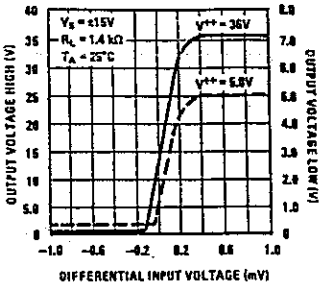
Input Currents



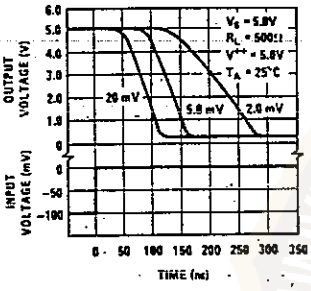
Supply Currents



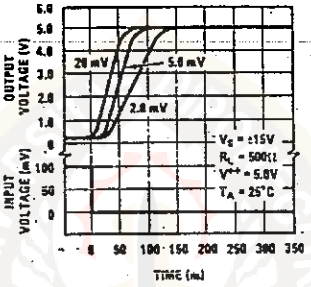
Transfer Function



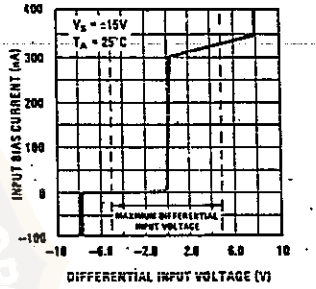
Response Time for Various Input Overdrives



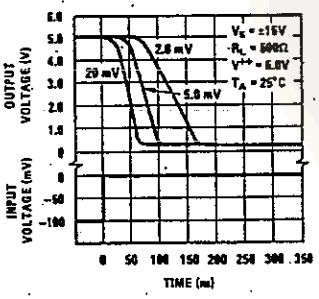
Response Time for Various Input Overdrives



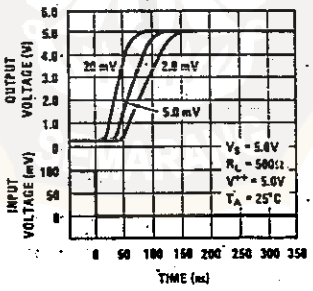
Input Characteristics



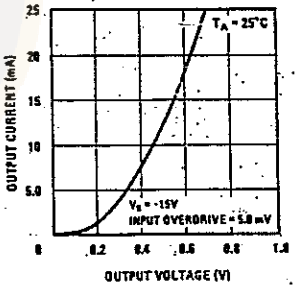
Response Time for Various Input Overdrives



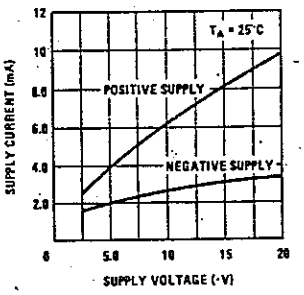
Response Time for Various Input Overdrives



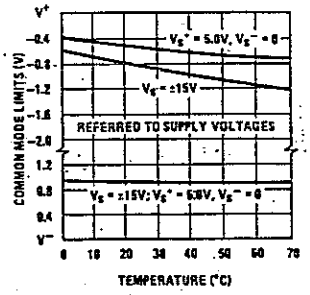
Output Saturation Voltage



Supply Current



Common Mode Limits



Output Limiting Characteristics