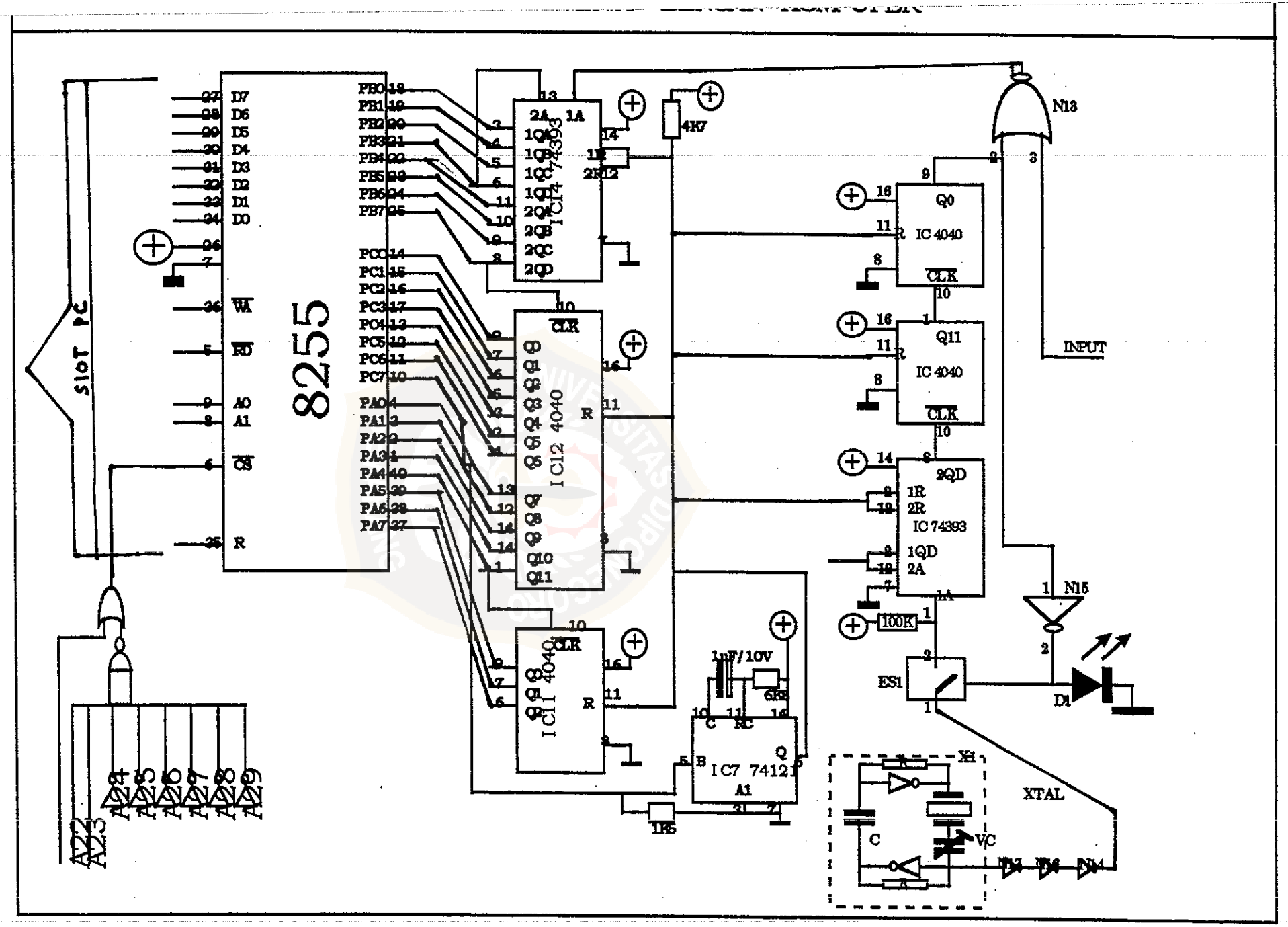


```
program counter;
uses crt,graph,grafik;
var E,F,G,V,W : real;
    pilih : char;
    done : boolean;
    dtx:string[10];
const portA = $300;
      portB = $301;
      portC = $302;
      portD = $303;

procedure hitung1;
begin
port[$303] := $93;
port[$302] := $80;
port[$302] := $0;
port[$303] := $9b;

delay(500);

E := port[$300];
F := port[$301];
G := port[$302];

V := 32768*E+256*F+G;
W := V/0.262;
settextstyle(smallfont,horizdir,6);
str(W:10:5,dtx);
outtextxy(getmaxx - 200, 200,dtx);
end;

procedure hitung2;
begin
port[$303] := $93;
port[$302] := $80;
port[$302] := $0;
port[$303] := $9b;

delay(500);

E := port[$300];
F := port[$301];
G := port[$302];

V := 32768*E+256*F+G;
W := (V/0.262)/1000;
settextstyle(smallfont,horizdir,6);
str(W:10:5,dtx);
outtextxy(getmaxx - 200, 200,dtx);
end;

procedure hitung3;
```

```
begin
port[$303] := $93;
port[$302] := $80;
port[$302] := $0;
port[$303] := $9b;

delay(500);

E := port[$300];
F := port[$301];
G := port[$302];

V := 32768*E+256*F+G;
W := (V/0.262)/1000000;
settextstyle(smallfont,horizdir,6);
str(W:10:5,dtx);
outtextxy(getmaxx - 200, 200,dtx);
end;

procedure tampil;
begin
buka;
rectangle(0,0,630,400);
rectangle(60,60,575,20);
rectangle(60,370,575,350);
settextstyle(smallfont,horizdir,8);
settextjustify(centertext,righttext);
outtextxy(getmaxx div 2, 30,'PENGUKUR FREKUENSI DI KONTROL
PC');
settextstyle(smallfont,horizdir,6);
outtextxy(getmaxx div 2, 350,'H (Hz)   K (KHz)   M (MHz)   ESC
(QUIT)');
outtextxy(getmaxx div 2, 369,'RAHENDRA J 401910656');
end;

procedure menu;
begin
done := false;
pilih := readkey;
repeat
begin
case pilih of
#104 : begin
          outtextxy(getmaxx div 3, 200,'FREKUENSI TERUKUR
(HZ)');
          hitung1;
          repeat until readkey = #27;
          end;
#107 : begin
          outtextxy(getmaxx div 3, 200,'FREKUENSI TERUKUR
(KHZ)');
          hitung2;
```

```
            repeat until readkey = #27;
            end;
#109 : begin
            outtextxy(getmaxx div 3, 200,'FREKUENSI TERUKUR
(MHZ)');
            hitung3;
            repeat until readkey = #27;
            end;
#115  : begin
            menu;
      end;
end;
end;
until readkey=#27;
end;

begin
tampil;
menu;
tutup;
end.

unit grafik;
interface
uses
crt,graph;
procedure buka;
procedure tutup;

implementation
procedure buka;
var
gd,gm,errorcode:integer;
begin
gd := vgalo;
initgraph (gd,gm,'');
errorcode := graphresult;
if errorcode <> grok then halt;
end;

procedure tutup;
begin
closegraph;
end;
end.
```

National Semiconductor

February 1988

# CD4020BM/CD4020BC 14-Stage Ripple Carry Binary Counters CD4040BM/CD4040BC 12-Stage Ripple Carry Binary Counters CD4060BM/CD4060BC 14-Stage Ripple Carry Binary Counters

## General Description

The CD4020BM/CD4020BC, CD4060BM/CD4060BC are 14-stage ripple carry binary counters, and the CD4040BM/CD4040BC is a 12-stage ripple carry binary counter. The counters are advanced one count on the negative transition of each clock pulse. The counters are reset to the zero state by a logical "1" at the reset input independent of clock.

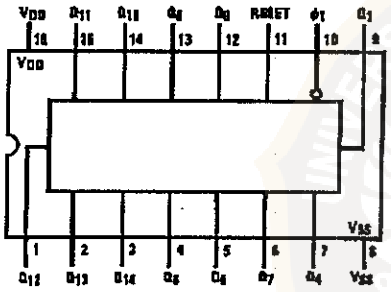
## Features

- Wide supply voltage range — 1.0V to 15V
- High noise immunity — 0.45 $V_{DD}$ (typ.)
- Low power TTL compatibility — Fan out of 2 driving 74L or 1 driving 74LS
- Medium speed operation — 8 MHz typ. at $V_{DD}$ = 10V
- Schmitt trigger clock input

## Connection Diagrams

Dual-In-Line Package

CD4020BM/CD4020BC

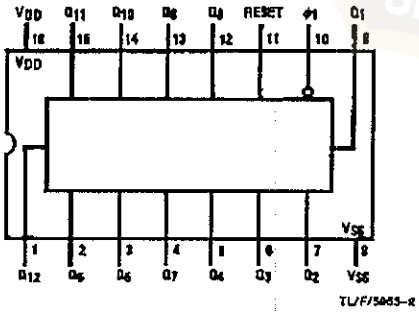



Top View

Order Number CD4020B, CD4040B or CD4060B

Dual-In-Line Package

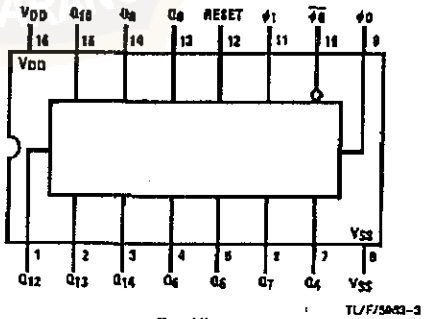
CD4040BM/CD4040BC




Top View

Dual-In-Line Package

CD4060BM/CD4060BC




Top View



RRD-B30M106/Printed in U. S. A.

## DC Electrical Characteristics 40XXBC (Note 2) (Continued)

| Symbol | Parameter | Conditions | −40°C | | +25°C | | | +85°C | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Typ | Max | Min | Max | |
| $V_{OH}$ | High Level Output Voltage | $V_{DD}$ = 5V | 4.95 | | 4.95 | 5 | | 4.95 | | V |
| | | $V_{DD}$ = 10V | 9.95 | | 9.95 | 10 | | 9.95 | | V |
| | | $V_{DD}$ = 15V | 14.95 | | 14.95 | 15 | | 14.95 | | V |
| $V_{IL}$ | Low Level Input Voltage | $V_{DD}$ = 5V, $V_O$ = 0.5V or 4.5V | | 1.5 | | 2 | 1.5 | | 1.5 | V |
| | | $V_{DD}$ = 10V, $V_O$ = 1.0V or 9.0V | | 3.0 | | 4 | 3.0 | | 3.0 | V |
| | | $V_{DD}$ = 15V, $V_O$ = 1.5V or 13.5V | | 4.0 | | 6 | 4.0 | | 4.0 | V |
| $V_{IH}$ | High Level Input Voltage | $V_{DD}$ = 5V, $V_O$ = 0.5V or 4.5V | 3.5 | | 3.5 | 3 | | 3.5 | | V |
| | | $V_{DD}$ = 10V, $V_O$ = 1.0V or 9.0V | 7.0 | | 7.0 | 6 | | 7.0 | | V |
| | | $V_{DD}$ = 15V, $V_O$ = 1.5V or 13.5V | 11.0 | | 11.0 | 9 | | 11.0 | | V |
| $I_{OL}$ | Low Level Output Current (See Note 3) | $V_{DD}$ = 5V, $V_O$ = 0.4V | 0.52 | | 0.44 | 0.88 | | 0.36 | | mA |
| | | $V_{DD}$ = 10V, $V_O$ = 0.5V | 1.3 | | 1.1 | 2.25 | | 0.9 | | mA |
| | | $V_{DD}$ = 15V, $V_O$ = 1.5V | 3.6 | | 3.0 | 8.8 | | 2.4 | | mA |
| $I_{OH}$ | High Level Output Current (See Note 3) | $V_{DD}$ = 5V, $V_O$ = 4.6V | −0.52 | | −0.44 | −0.88 | | −0.36 | | mA |
| | | $V_{DD}$ = 10V, $V_O$ = 9.5V | −1.3 | | −1.1 | −2.25 | | −0.9 | | mA |
| | | $V_{DD}$ = 15V, $V_O$ = 13.5V | −3.6 | | −3.0 | −8.8 | | −2.4 | | mA |
| $I_{IN}$ | Input Current | $V_{DD}$ = 15V, $V_{IN}$ = 0V | | 0.30 | | $10^{-5}$ | 0.30 | | 1.0 | μA |
| | | $V_{DD}$ = 15V, $V_{IN}$ = 15V | | 0.30 | | $10^{-5}$ | 0.30 | | 1.0 | μA |

## AC Electrical Characteristics* CD4020BM/CD4020BC, CD4040BM/CD4040BC

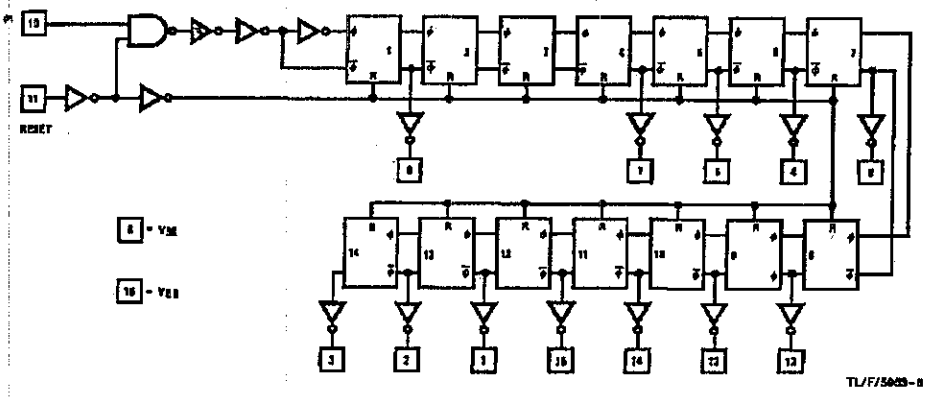
$T_A$ = 25°C, $C_L$ = 50 pF, $R_L$ = 200k, $t_r$ = $t_f$ = 20 ns, unless otherwise noted

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{PHL1}$, $t_{PLH1}$ | Propagation Delay Time to $Q_1$ | $V_{DD}$ = 5V | | 250 | 550 | ns |
| | | $V_{DD}$ = 10V | | 100 | 210 | ns |
| | | $V_{DD}$ = 15V | | 75 | 150 | ns |
| $t_{PHL}$, $t_{PLH}$ | Interstage Propagation Delay Time from $Q_n$ to $Q_{n+1}$ | $V_{DD}$ = 5V | | 150 | 330 | ns |
| | | $V_{DD}$ = 10V | | 60 | 125 | ns |
| | | $V_{DD}$ = 15V | | 45 | 90 | ns |
| $t_{THL}$, $t_{TLH}$ | Transition Time | $V_{DD}$ = 5V | | 100 | 200 | ns |
| | | $V_{DD}$ = 10V | | 50 | 100 | ns |
| | | $V_{DD}$ = 15V | | 40 | 80 | ns |
| $t_{WL}$, $t_{WH}$ | Minimum Clock Pulse Width | $V_{DD}$ = 5V | | 125 | 335 | ns |
| | | $V_{DD}$ = 10V | | 50 | 125 | ns |
| | | $V_{DD}$ = 15V | | 40 | 100 | ns |
| $t_{rCL}$, $t_{fCL}$ | Maximum Clock Rise and Fall Time | $V_{DD}$ = 5V | | | No Limit | ns |
| | | $V_{DD}$ = 10V | | | No Limit | ns |
| | | $V_{DD}$ = 15V | | | No Limit | ns |
| $f_{CL}$ | Maximum Clock Frequency | $V_{DD}$ = 5V | 1.5 | 4 | | MHz |
| | | $V_{DD}$ = 10V | 4 | 10 | | MHz |
| | | $V_{DD}$ = 15V | 5 | 12 | | MHz |
| $t_{PHL(R)}$ | Reset Propagation Delay | $V_{DD}$ = 5V | | 200 | 450 | ns |
| | | $V_{DD}$ = 10V | | 100 | 210 | ns |
| | | $V_{DD}$ = 15V | | 80 | 170 | ns |
| $t_{WH(R)}$ | Minimum Reset Pulse Width | $V_{DD}$ = 5V | | 200 | 450 | ns |
| | | $V_{DD}$ = 10V | | 100 | 210 | ns |
| | | $V_{DD}$ = 15V | | 80 | 170 | ns |
| $C_{in}$ | Average Input Capacitance | Any Input | | 5 | 7.5 | pF |
| $C_{pd}$ | Power Dissipation Capacitance | | | 50 | | pF |

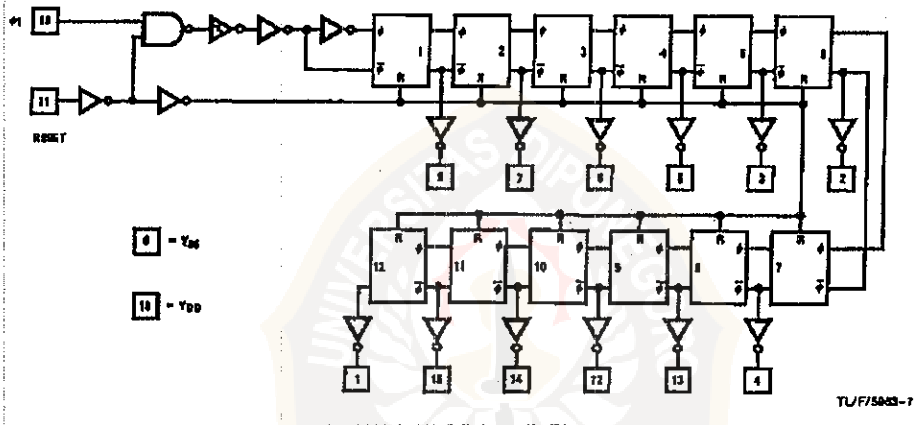
*AC Parameters are guaranteed by DC correlated testing.

## Schematic Diagrams

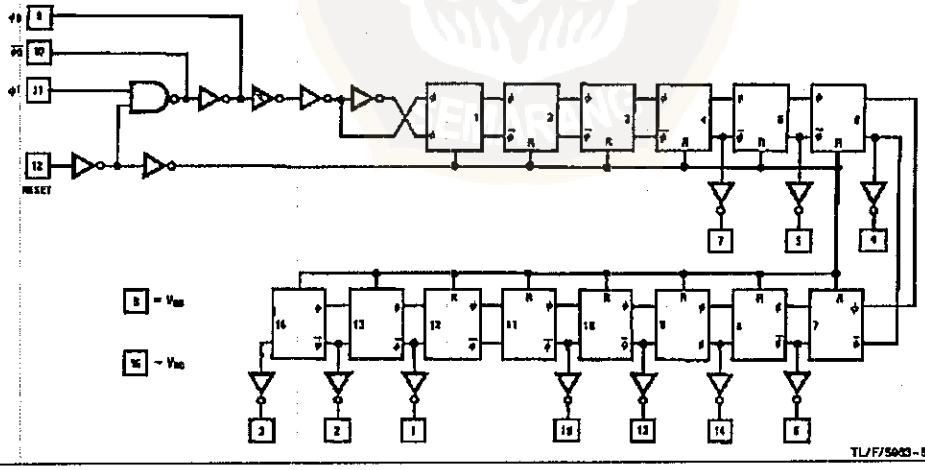
CD4020BM/CD4020BC Schematic Diagram




CD4040BM/CD4040BC Schematic Diagram




CD4060BM/CD4060BC Schematic Diagram



National Semiconductor

June 1989

# 54121/DM54121/DM74121 One-Shot with Clear and Complementary Outputs

## General Description

The DM54/74121 is a monostable multivibrator featuring both positive and negative edge triggering with complementary outputs. An internal 2kΩ timing resistor is provided for design convenience minimizing component count and layout problems. This device can be used with a single external capacitor. Inputs (A) are active-low trigger transition inputs and input (B) is an active-high transition Schmitt-trigger input that allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second. A high immunity to $V_{CC}$ noise of typically 1.5V is also provided by internal circuitry at the input stage.

To obtain optimum and trouble free operation please read operating rules and NSC one-shot application notes carefully and observe recommendations.

## Features

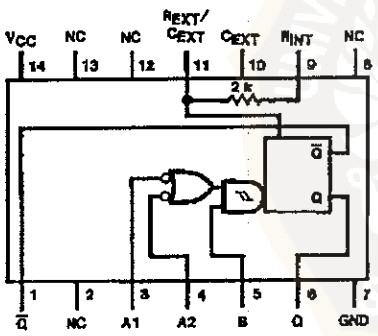
- Triggered from active-high transition or active-low transition inputs
- Variable pulse width from 30 ns to 28 seconds
- Jitter free Schmitt-trigger input
- Excellent noise immunity typically 1.2V
- Stable pulse width up to 90% duty cycle
- TTL, DTL compatible
- Compensated for $V_{CC}$ and temperature variations
- Input clamp diodes
- Alternate Military/Aerospace device (54121) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

## Functional Description

The basic output pulse width is determined by selection of an internal resistor $R_{INT}$ or an external resistor ($R_X$) and capacitor ($C_X$). Once triggered the output pulse width is independent of further transitions of the inputs and is a function of the timing components. Pulse width can vary from a few nano-seconds to 28 seconds by choosing appropriate $R_X$ and $C_X$ combinations. There are three trigger inputs from the device, two negative edge-triggering (A) inputs, one positive edge Schmitt-triggering (B) input.

## Connection Diagram

Dual-In-Line Package




TL/F/5338-1

Order Number 54121DMQB, 54121FMQB, DM54121J, DM54121W or DM74121N
See NS Package Number J14A, N14A or W14B

## Function Table

| Inputs | | | Outputs | |
|---|---|---|---|---|
| A1 | A2 | B | Q | Q̄ |
| L | X | H | L | H |
| X | L | H | L | H |
| X | X | L | L | H |
| H | H | X | L | H |
| H | ↓ | H | ⎍ | ⎏ |
| ↓ | H | H | ⎍ | ⎏ |
| ↓ | ↓ | H | ⎍ | ⎏ |
| L | X | ↑ | ⎍ | ⎏ |
| X | L | ↑ | ⎍ | ⎏ |

H = High Logic Level
L = Low Logic Level
X = Can Be Either Low or High
↑ = Positive Going Transition
↓ = Negative Going Transition
⎍ = A Positive Pulse
⎏ = A Negative Pulse



RRD-B30M105/Printed in U. S. A.

National Semiconductor

June 1989

# DM74LS393 Dual 4-Bit Binary Counter

## General Description

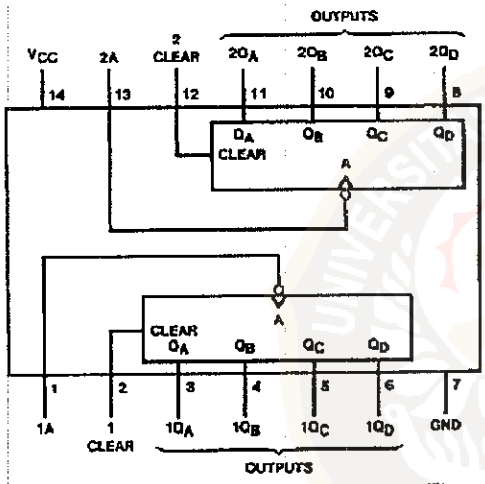
Each of these monolithic circuits contains eight master-slave flip-flops and additional gating to implement two individual four-bit counters in a single package. The 'LS393 comprises two independent four-bit binary counters each having a clear and a clock input. N-bit binary counters can be implemented with each package providing the capability of divide-by-256. The LS393 has parallel outputs from each counter stage so that any submultiple of the input count freqency is available for system-timing signals.

## Features

- Dual version of the popular 'LS93
- 'LS393 dual 4-bit binary counter with individual clocks
- Direct clear for each 4-bit counter
- Dual 4-bit versions can significantly improve system densities by reducing counter package count by 50%
- Typical maximum count frequency 35 MHz
- Buffered outputs reduce possibility of collector commutation

## Connection Diagram

Dual-In-Line Package




TL/F/6434-1

Order Number DM74LS393M or DM74LS393N
See NS Package Number M14A or N14A

## Function Table

Count Sequence
(Each Counter)

| Count | Outputs | | | |
|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |
| 10 | H | L | H | L |
| 11 | H | L | H | H |
| 12 | H | H | L | L |
| 13 | H | H | L | H |
| 14 | H | H | H | L |
| 15 | H | H | H | H |

H = High Logic Level
L = Low Logic Level



RRD-B30M106/Printed in U. S. A.

## Absolute Maximum Ratings (Note)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage | 7V |
| Input Voltage | |
| Clear | 7V |
| A | 5.5V |
| Operating Free Air Temperature Range | |
| DM74LS | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C |

*Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

## Recommended Operating Conditions

| Symbol | Parameter | | DM74LS393 | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC}$ | Supply Voltage | | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | High Level Input Voltage | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | | 0.8 | V |
| $I_{OH}$ | High Level Output Current | | | | 0.4 | mA |
| $I_{OL}$ | Low Level Output Current | | | | 8 | mA |
| $f_{CLK}$ | Clock Frequency (Note 1) | | 0 | | 25 | MHz |
| $f_{CLK}$ | Clock Frequency (Note 2) | | 0 | | 20 | MHz |
| $t_W$ | Pulse Width (Note 7) | A | 20 | | | ns |
| | | Clear High | 20 | | | |
| $t_{REL}$ | Clear Release Time (Notes 3 & 7) | | 25 ↓ | | | ns |
| $T_A$ | Free Air Operating Temperature | | 0 | | 70 | °C |

## Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions | | Min | Typ (Note 4) | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −18 mA | | | | 1.5 | V |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $I_{OH}$ = Max, $V_{IL}$ = Max, $V_{IH}$ = Min | | 2.7 | 3.4 | | V |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $I_{OL}$ = Max, $V_{IL}$ = Max, $V_{IH}$ = Min | | | 0.35 | 0.5 | V |
| | | $I_{OL}$ = 4 mA, $V_{CC}$ = Min | | | 0.25 | 0.4 | |
| $I_I$ | Input Current @ Max Input Voltage | $V_{CC}$ = Max, $V_I$ = 7V | Clear | | | 0.1 | mA |
| | | $V_{CC}$ = Max, $V_I$ = 5.5V | A | | | 0.2 | |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.7V | Clear | | | 20 | μA |
| | | | A | | | 40 | |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4V | Clear | | | 0.4 | mA |
| | | | A | | | 1.6 | |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (Note 5) | | −20 | | −100 | mA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = Max (Note 6) | | | 15 | 26 | mA |

Note 1: $C_L$ = 15 pF, $R_L$ = 2 kΩ, $T_A$ = 25°C and $V_{CC}$ = 5V.

Note 2: $C_L$ = 50 pF, $R_L$ = 2 kΩ, $T_A$ = 25°C and $V_{CC}$ = 5V.

Note 3: The symbol (↓) indicates that the falling edge of the clear pulse is used for reference.

Note 4: All typicals are at $V_{CC}$ = 5V, $T_A$ = 25°C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

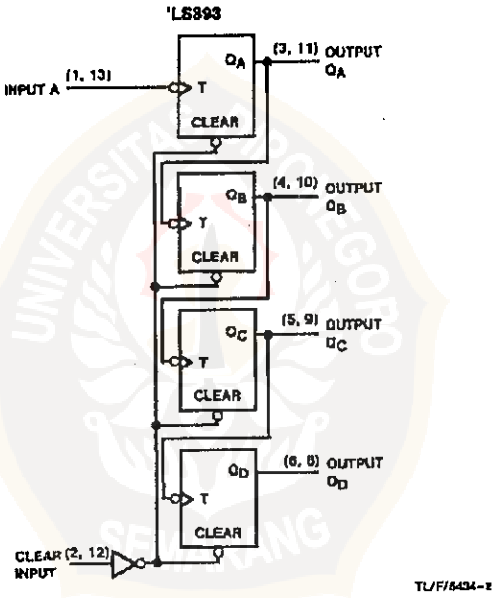
Note 6: $I_{CC}$ is measured with all outputs open, both CLEAR inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

Note 7: $T_A$ = 25°C, and $V_{CC}$ = 5V.

## Switching Characteristics at $V_{CC}$ = 5V and $T_A$ = 25°C (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | From (Input) To (Output) | $R_L$ = 2 kΩ | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | $C_L$ = 15 pF | | $C_L$ = 50 pF | | |
| | | | Min | Max | Min | Max | |
| $f_{MAX}$ | Maximum Clock Frequency | A to $Q_A$ | 25 | | 20 | | MHz |
| $t_{PLH}$ | Propagation Delay Time Low to High Level Output | A to $Q_A$ | | 20 | | 24 | ns |
| $t_{PHL}$ | Propagation Delay Time High to Low Level Output | A to $Q_A$ | | 20 | | 30 | ns |
| $t_{PLH}$ | Propagation Delay Time Low to High Level Output | A to $Q_D$ | | 60 | | 87 | ns |
| $t_{PHL}$ | Propagation Delay Time High to Low Level Output | A to $Q_D$ | | 60 | | 87 | ns |
| $t_{PHL}$ | Propagation Delay Time High to Low Level Output | Clear to Any Q | | 39 | | 45 | ns |

## Logic Diagram



MOTOROLA

# DUAL DECADE COUNTER; DUAL 4-STAGE BINARY COUNTER

**SN54/74LS390**
**SN54/74LS393**

**DUAL DECADE COUNTER; DUAL 4-STAGE BINARY COUNTER**

**LOW POWER SCHOTTKY**

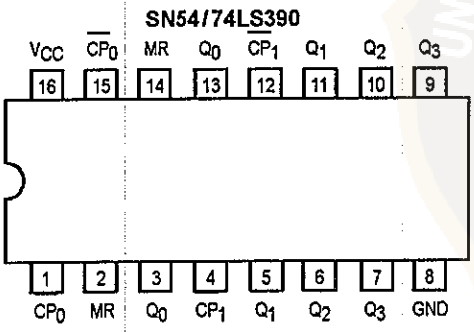
The SN54/74LS390 and SN54/74LS393 each contain a pair of high-speed 4-stage ripple counters. Each half of the LS390 is partitioned into a divide-by-two section and a divide-by five section, with a separate clock input for each section. The two sections can be connected to count in the 8.4.2.1 BCD code or they can count in a biquinary sequence to provide a square wave (50% duty cycle) at the final output.

Each half of the LS393 operates as a Modulo-16 binary divider, with the last three stages triggered in a ripple fashion. In both the LS390 and the LS393, the flip-flops are triggered by a HIGH-to-LOW transition of their CP inputs. Each half of each circuit type has a Master Reset input which responds to a HIGH signal by forcing all four outputs to the LOW state.

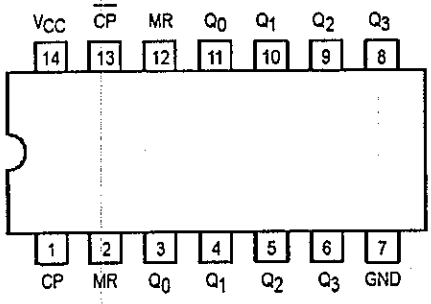
- Dual Versions of LS290 and LS293
- LS390 has Separate Clocks Allowing ÷2, ÷2.5, ÷5
- Individual Asynchronous Clear for Each Counter
- Typical Max Count Frequency of 50 MHz
- Input Clamp Diodes Minimize High Speed Termination Effects

**CONNECTION DIAGRAM DIP** (TOP VIEW)

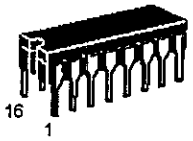
**SN54/74LS390**



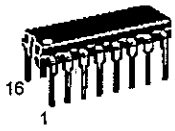

**SN54/74LS393**



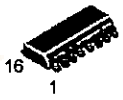

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.



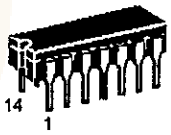

J SUFFIX
CERAMIC
CASE 620-09



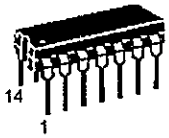

N SUFFIX
PLASTIC
CASE 648-08



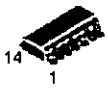

D SUFFIX
SOIC
CASE 751B-03




J SUFFIX
CERAMIC
CASE 632-08




N SUFFIX
PLASTIC
CASE 646-06




D SUFFIX
SOIC
CASE 751A-02

**ORDERING INFORMATION**

| | |
|---|---|
| SN54LSXXXJ | Ceramic |
| SN74LSXXXN | Plastic |
| SN74LSXXXD | SOIC |

| PIN NAMES | | LOADING (Note a) HIGH | LOW |
|---|---|---|---|
| $\overline{CP}$ | Clock (Active LOW going edge) Input to ÷16 (LS393) | 0.5 U.L. | 1.0 U.L. |
| $\overline{CP_0}$ | Clock (Active LOW going edge) Input to ÷2 (LS390) | 0.5 U.L. | 1.0 U.L. |
| $\overline{CP_1}$ | Clock (Active LOW going edge) Input to ÷5 (LS390) | 0.5 U.L. | 1.5 U.L. |
| MR | Master Reset (Active HIGH) Input | 0.5 U.L. | 0.25 U.L. |
| $Q_0-Q_3$ | Flip-Flop outputs (Note b) | 10 U.L. | 5 (2.5) U.L. |

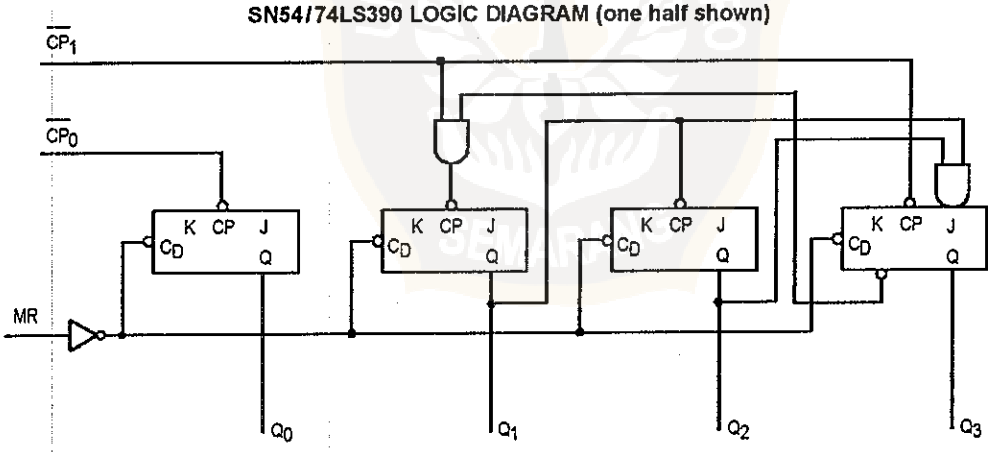
NOTES:
a) 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

## FUNCTIONAL DESCRIPTION

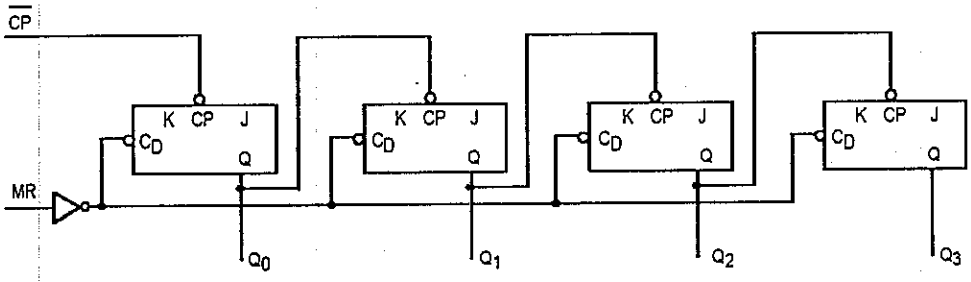
Each half of the SN54/74LS393 operates in the Modulo 16 binary sequence, as indicated in the ÷16 Truth Table. The first flip-flop is triggered by HIGH-to-LOW transitions of the CP input signal. Each of the other flip-flops is triggered by a HIGH-to-LOW transition of the Q output of the preceding flip-flop. Thus state changes of the Q outputs do not occur simultaneously. This means that logic signals derived from combinations of these outputs will be subject to decoding spikes and, therefore, should not be used as clocks for other counters, registers or flip-flops. A HIGH signal on MR forces all outputs to the LOW state and prevents counting.

Each half of the LS390 contains a ÷5 section that is independent except for the common MR function. The ÷5 section operates in 4.2.1 binary sequence, as shown in the ÷5 Truth Table, with the third stage output exhibiting a 20% duty cycle when the input frequency is constant. To obtain a ÷10 function having a 50% duty cycle output, connect the input signal to $CP_1$ and connect the $Q_3$ output to the $CP_0$ input; the $Q_0$ output provides the desired 50% duty cycle output. If the input frequency is connected to $CP_0$ and the $Q_0$ output is connected to $CP_1$, a decade divider operating in the 8.4.2.1 BCD code is obtained, as shown in the BCD Truth Table. Since the flip-flops change state asynchronously, logic signals derived from combinations of LS390 outputs are also subject to decoding spikes. A HIGH signal on MR forces all outputs LOW and prevents counting.

SN54/74LS390 LOGIC DIAGRAM (one half shown)




SN54/74LS393 LOGIC DIAGRAM (one half shown)



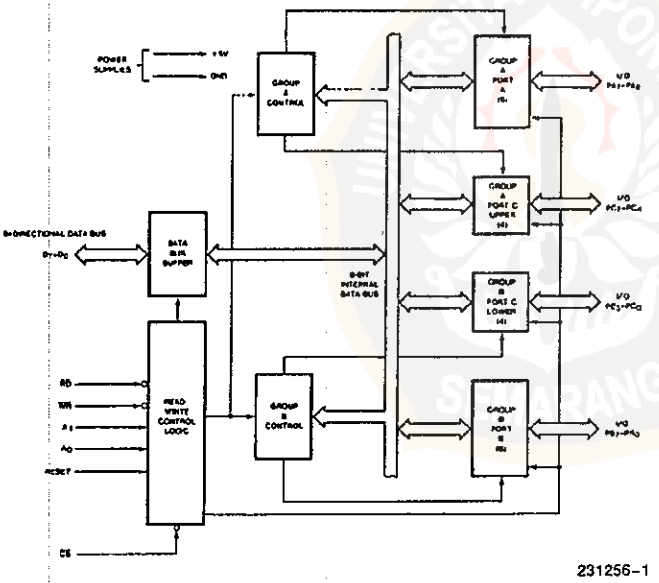
# 82C55A
# CHMOS PROGRAMMABLE PERIPHERAL INTERFACE

- Compatible with all Intel and Most Other Microprocessors
- High Speed, "Zero Wait State" Operation with 8 MHz 8086/88 and 80186/188
- 24 Programmable I/O Pins
- Low Power CHMOS
- Completely TTL Compatible
- Control Word Read-Back Capability
- Direct Bit Set/Reset Capability
- 2.5 mA DC Drive Capability on all I/O Port Outputs
- Available in 40-Pin DIP and 44-Pin PLCC
- Available in EXPRESS
  - Standard Temperature Range
  - Extended Temperature Range

The Intel 82C55A is a high-performance, CHMOS version of the industry standard 8255A general purpose programmable I/O device which is designed for use with all Intel and most other microprocessors. It provides 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. The 82C55A is pin compatible with the NMOS 8255A and 8255A-5.

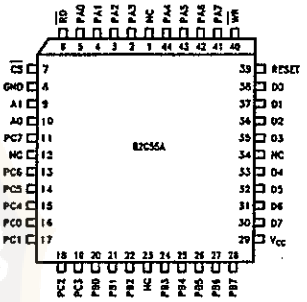
In MODE 0, each group of 12 I/O pins may be programmed in sets of 4 and 8 to be inputs or outputs. In MODE 1, each group may be programmed to have 8 lines of input or output. 3 of the remaining 4 pins are used for handshaking and interrupt control signals. MODE 2 is a strobed bi-directional bus configuration.

The 82C55A is fabricated on Intel's advanced CHMOS III technology which provides low power consumption with performance equal to or greater than the equivalent NMOS product. The 82C55A is available in 40-pin DIP and 44-pin plastic leaded chip carrier (PLCC) packages.

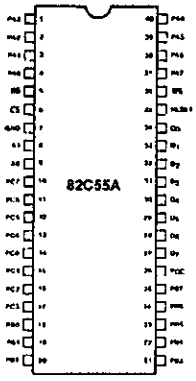



231256-1

**Figure 1. 82C55A Block Diagram**




231256-31




231256-2

**Figure 2. 82C55A Pinout**

Diagrams are for pin reference only. Package sizes are not to scale.

October 1995

Order Number: 231256-004

**Table 1. Pin Description**

| Symbol | Pin Number Dip | Pin Number PLCC | Type | Name and Function |
|---|---|---|---|---|
| $PA_{3-0}$ | 1–4 | 2–5 | I/O | **PORT A, PINS 0–3:** Lower nibble of an 8-bit data output latch/buffer and an 8-bit data input latch. |
| $\overline{RD}$ | 5 | 6 | I | **READ CONTROL:** This input is low during CPU read operations. |
| $\overline{CS}$ | 6 | 7 | I | **CHIP SELECT:** A low on this input enables the 82C55A to respond to $\overline{RD}$ and $\overline{WR}$ signals. $\overline{RD}$ and WR are ignored otherwise. |
| GND | 7 | 8 | | **System Ground** |
| $A_{1-0}$ | 8–9 | 9–10 | I | **ADDRESS:** These input signals, in conjunction $\overline{RD}$ and $\overline{WR}$, control the selection of one of the three ports or the control word registers. |

| $A_1$ | $A_0$ | $\overline{RD}$ | $\overline{WR}$ | $\overline{CS}$ | Input Operation (Read) |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | Port A - Data Bus |
| 0 | 1 | 0 | 1 | 0 | Port B - Data Bus |
| 1 | 0 | 0 | 1 | 0 | Port C - Data Bus |
| 1 | 1 | 0 | 1 | 0 | Control Word - Data Bus |
| | | | | | **Output Operation (Write)** |
| 0 | 0 | 1 | 0 | 0 | Data Bus - Port A |
| 0 | 1 | 1 | 0 | 0 | Data Bus - Port B |
| 1 | 0 | 1 | 0 | 0 | Data Bus - Port C |
| 1 | 1 | 1 | 0 | 0 | Data Bus - Control |
| | | | | | **Disable Function** |
| X | X | X | X | 1 | Data Bus - 3 - State |
| X | X | 1 | 1 | 0 | Data Bus - 3 - State |

| Symbol | Pin Number Dip | Pin Number PLCC | Type | Name and Function |
|---|---|---|---|---|
| $PC_{7-4}$ | 10–13 | 11,13–15 | I/O | **PORT C, PINS 4–7:** Upper nibble of an 8-bit data output latch/buffer and an 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B. |
| $PC_{0-3}$ | 14–17 | 16–19 | I/O | **PORT C, PINS 0–3:** Lower nibble of Port C. |
| $PB_{0-7}$ | 18–25 | 20–22, 24–28 | I/O | **PORT B, PINS 0–7:** An 8-bit data output latch/buffer and an 8-bit data input buffer. |
| $V_{CC}$ | 26 | 29 | | **SYSTEM POWER:** + 5V Power Supply. |
| $D_{7-0}$ | 27–34 | 30–33, 35–38 | I/O | **DATA BUS:** Bi-directional, tri-state data bus lines, connected to system data bus. |
| RESET | 35 | 39 | I | **RESET:** A high on this input clears the control register and all ports are set to the input mode. |
| $\overline{WR}$ | 36 | 40 | I | **WRITE CONTROL:** This input is low during CPU write operations. |
| $PA_{7-4}$ | 37–40 | 41–44 | I/O | **PORT A, PINS 4–7:** Upper nibble of an 8-bit data output latch/buffer and an 8-bit data input latch. |
| NC | | 1, 12, 23, 34 | | No Connect |

## 82C55A FUNCTIONAL DESCRIPTION

### General

The 82C55A is a programmable peripheral interface device designed for use in Intel microcomputer systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer system bus. The functional configuration of the 82C55A is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

### Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the 82C55A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

### Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

### Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 82C55A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 82C55A.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A - Port A and Port C upper (C7–C4)
Control Group B - Port B and Port C lower (C3–C0)

The control word register can be both written and read as shown in the address decode table in the pin descriptions. Figure 6 shows the control word format for both Read and Write operations. When the control word is read, bit D7 will always be a logic "1", as this implies control word mode information.

### Ports A, B, and C

The 82C55A contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 82C55A.

**Port A.** One 8-bit data output latch/buffer and one 8-bit input latch buffer. Both "pull-up" and "pull-down" bus hold devices are present on Port A.

**Port B.** One 8-bit data input/output latch/buffer. Only "pull-up" bus hold devices are present on Port B.

**Port C.** One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B. Only "pull-up" bus hold devices are present on Port C.

See Figure 4 for the bus-hold circuit configuration for Port A, B, and C.

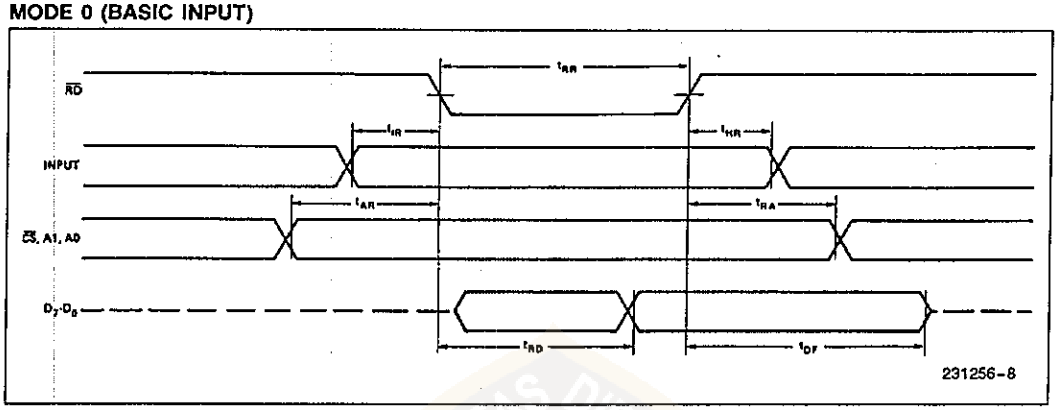
## Operating Modes

**Mode 0 (Basic Input/Output).** This functional configuration provides simple input and output operations for each of the three ports. No "handshaking" is required, data is simply written to or read from a specified port.

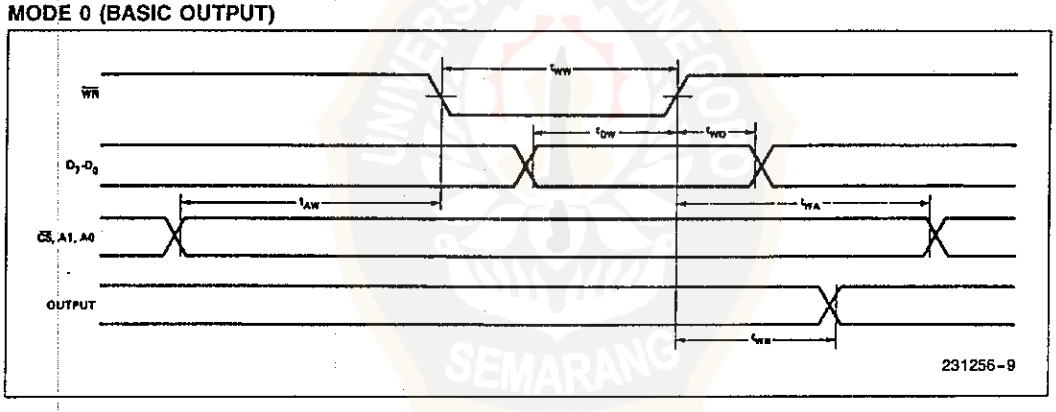
Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports.
- Any port can be input or output.
- Outputs are latched.
- Inputs are not latched.
- 16 different Input/Output configurations are possible in this Mode.

**MODE 0 (BASIC INPUT)**



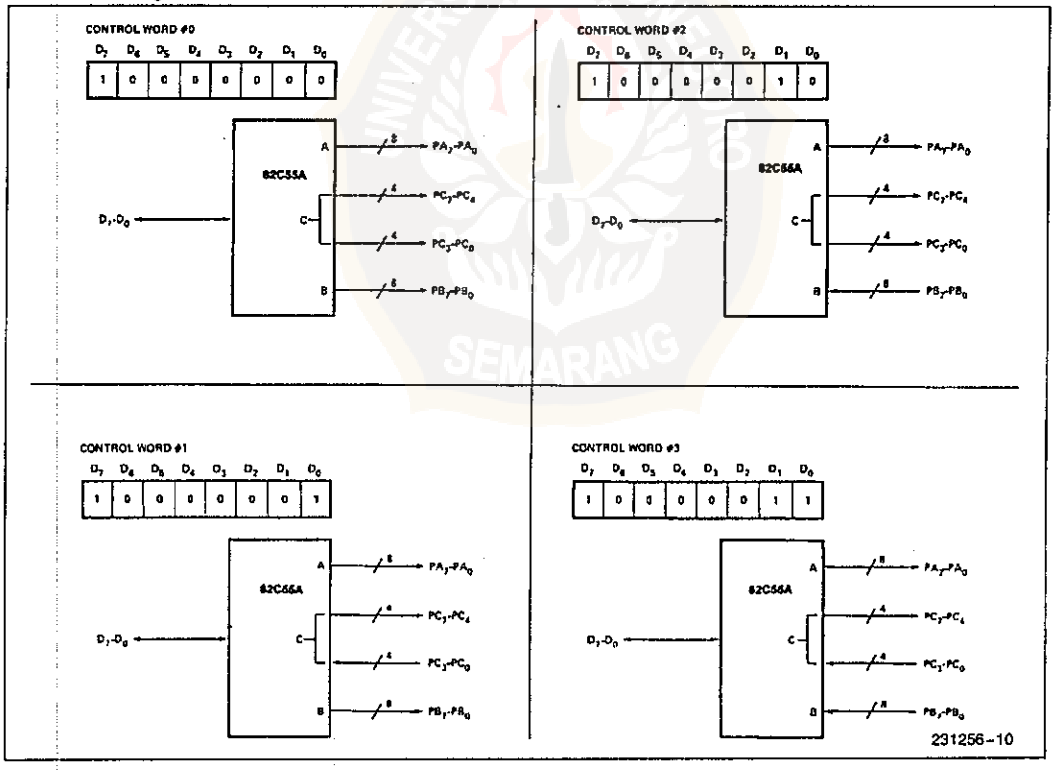

**MODE 0 (BASIC OUTPUT)**



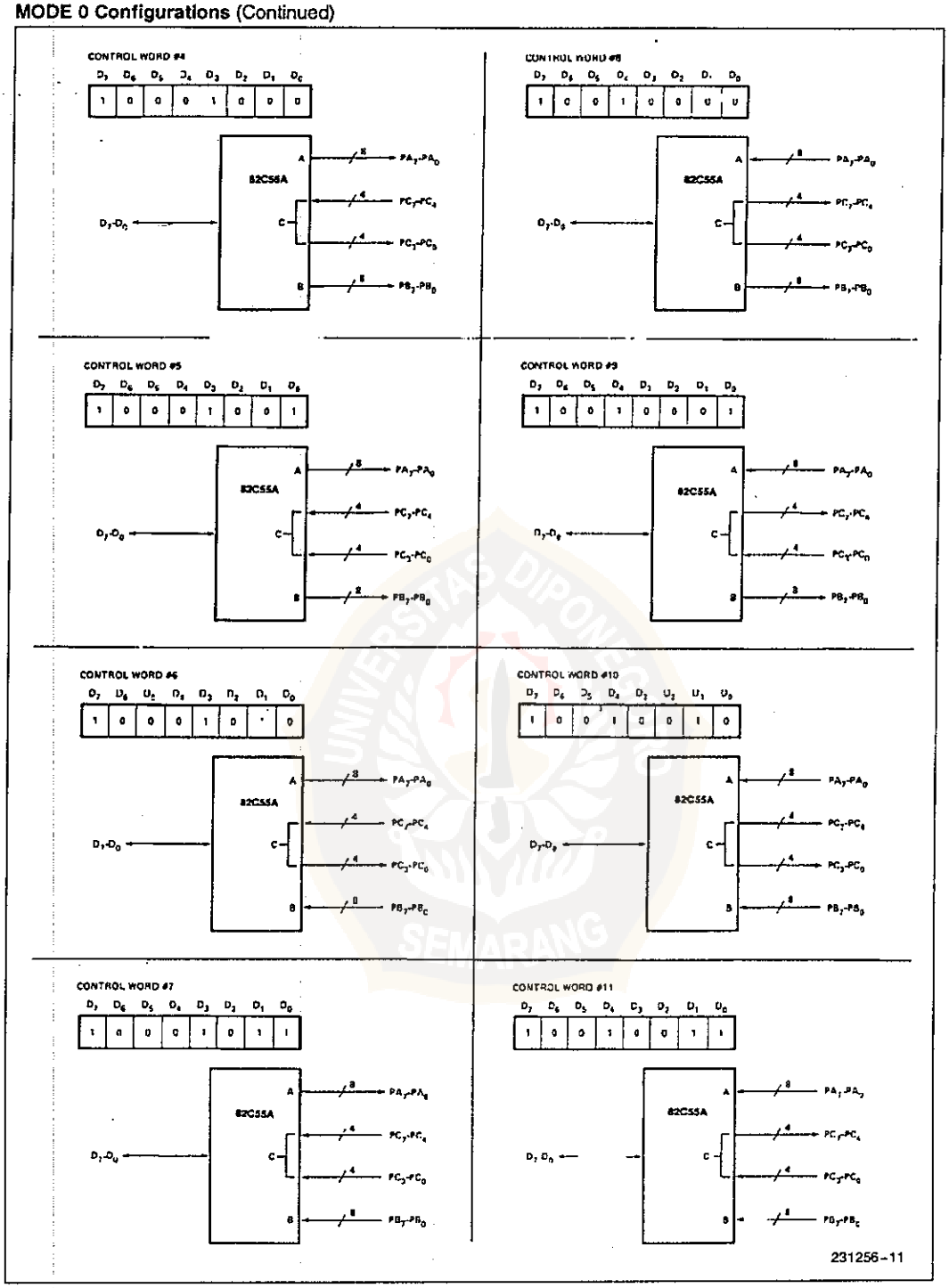
## MODE 0 Port Definition

| A | | B | | GROUP A | | | GROUP B | |
|---|---|---|---|---|---|---|---|---|
| $D_4$ | $D_3$ | $D_1$ | $D_0$ | PORT A | PORT C (UPPER) | # | PORT B | PORT C (LOWER) |
| 0 | 0 | 0 | 0 | OUTPUT | OUTPUT | 0 | OUTPUT | OUTPUT |
| 0 | 0 | 0 | 1 | OUTPUT | OUTPUT | 1 | OUTPUT | INPUT |
| 0 | 0 | 1 | 0 | OUTPUT | OUTPUT | 2 | INPUT | OUTPUT |
| 0 | 0 | 1 | 1 | OUTPUT | OUTPUT | 3 | INPUT | INPUT |
| 0 | 1 | 0 | 0 | OUTPUT | INPUT | 4 | OUTPUT | OUTPUT |
| 0 | 1 | 0 | 1 | OUTPUT | INPUT | 5 | OUTPUT | INPUT |
| 0 | 1 | 1 | 0 | OUTPUT | INPUT | 6 | INPUT | OUTPUT |
| 0 | 1 | 1 | 1 | OUTPUT | INPUT | 7 | INPUT | INPUT |
| 1 | 0 | 0 | 0 | INPUT | OUTPUT | 8 | OUTPUT | OUTPUT |
| 1 | 0 | 0 | 1 | INPUT | OUTPUT | 9 | OUTPUT | INPUT |
| 1 | 0 | 1 | 0 | INPUT | OUTPUT | 10 | INPUT | OUTPUT |
| 1 | 0 | 1 | 1 | INPUT | OUTPUT | 11 | INPUT | INPUT |
| 1 | 1 | 0 | 0 | INPUT | INPUT | 12 | OUTPUT | OUTPUT |
| 1 | 1 | 0 | 1 | INPUT | INPUT | 13 | OUTPUT | INPUT |
| 1 | 1 | 1 | 0 | INPUT | INPUT | 14 | INPUT | OUTPUT |
| 1 | 1 | 1 | 1 | INPUT | INPUT | 15 | INPUT | INPUT |

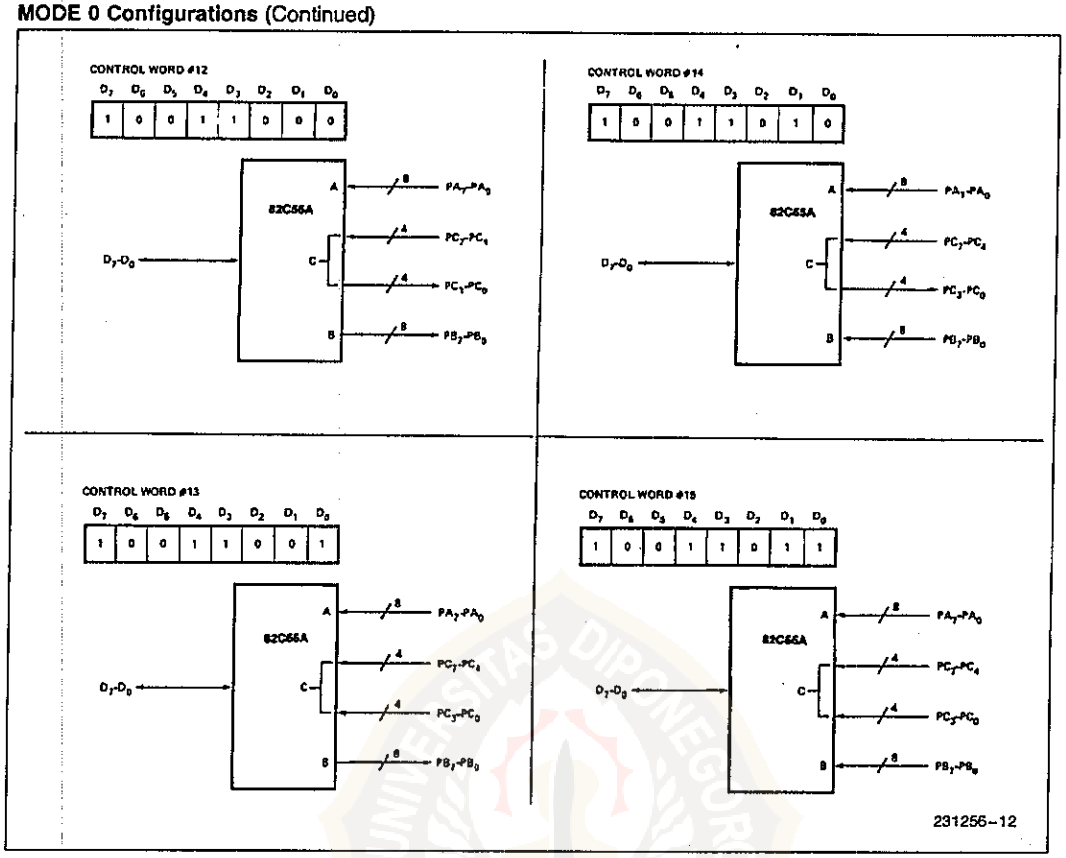
## MODE 0 Configurations



## MODE 0 Configurations (Continued)



**MODE 0 Configurations** (Continued)




## Operating Modes

**MODE 1 (Strobed Input/Output).** This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In mode 1, Port A and Port B use the lines on Port C to generate or accept these "handshaking" signals.

Mode 1 Basic functional Definitions:

- Two Groups (Group A and Group B).
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

## ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias....0°C to + 70°C
Storage Temperature .....− 65°C to + 150°C
Supply Voltage .....− 0.5 to + 8.0V
Operating Voltage .....+ 4V to + 7V
Voltage on any Input.....GND−2V to + 6.5V
Voltage on any Output ..GND−0.5V to $V_{CC}$ + 0.5V
Power Dissipation .....1 Watt

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

## D.C. CHARACTERISTICS

$T_A$ = 0°C to 70°C, $V_{CC}$ = +5V ±10%, GND = 0V ($T_A$ = −40°C to +85°C for Extended Temperture)

| Symbol | Parameter | Min | Max | Units | Test Conditions |
|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | −0.5 | 0.8 | V | |
| $V_{IH}$ | Input High Voltage | 2.0 | $V_{CC}$ | V | |
| $V_{OL}$ | Output Low Voltage | | 0.4 | V | $I_{OL}$ = 2.5 mA |
| $V_{OH}$ | Output High Voltage | 3.0<br>$V_{CC}$ − 0.4 | | V<br>V | $I_{OH}$ = −2.5 mA<br>$I_{OH}$ = −100 μA |
| $I_{IL}$ | Input Leakage Current | | ±1 | μA | $V_{IN}$ = $V_{CC}$ to 0V (Note 1) |
| $I_{OFL}$ | Output Float Leakage Current | | ±10 | μA | $V_{IN}$ = $V_{CC}$ to 0V (Note 2) |
| $I_{DAR}$ | Darlington Drive Current | ±2.5 | (Note 4) | mA | Ports A, B, C<br>$R_{ext}$ = 500Ω<br>$V_{ext}$ = 1.7V |
| $I_{PHL}$ | Port Hold Low Leakage Current | +50 | +300 | μA | $V_{OUT}$ = 1.0V<br>Port A only |
| $I_{PHH}$ | Port Hold High Leakage Current | −50 | −300 | μA | $V_{OUT}$ = 3.0V<br>Ports A, B, C |
| $I_{PHLO}$ | Port Hold Low Overdrive Current | −350 | | μA | $V_{OUT}$ = 0.8V |
| $I_{PHHO}$ | Port Hold High Overdrive Current | +350 | | μA | $V_{OUT}$ = 3.0V |
| $I_{CC}$ | $V_{CC}$ Supply Current | | 10 | mA | (Note 3) |
| $I_{CCSB}$ | $V_{CC}$ Supply Current-Standby | | 10 | μA | $V_{CC}$ = 5.5V<br>$V_{IN}$ = $V_{CC}$ or GND<br>Port Conditions<br>If I/P = Open/High<br>O/P = Open Only<br>With Data Bus = High/Low<br>$\overline{CS}$ = High<br>Reset = Low<br>Pure Inputs = Low/High |

**NOTES:**
1. Pins $A_1$, $A_0$, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, Reset.
2. Data Bus; Ports B, C.
3. Outputs open.
4. Limit output current to 4.0 mA.