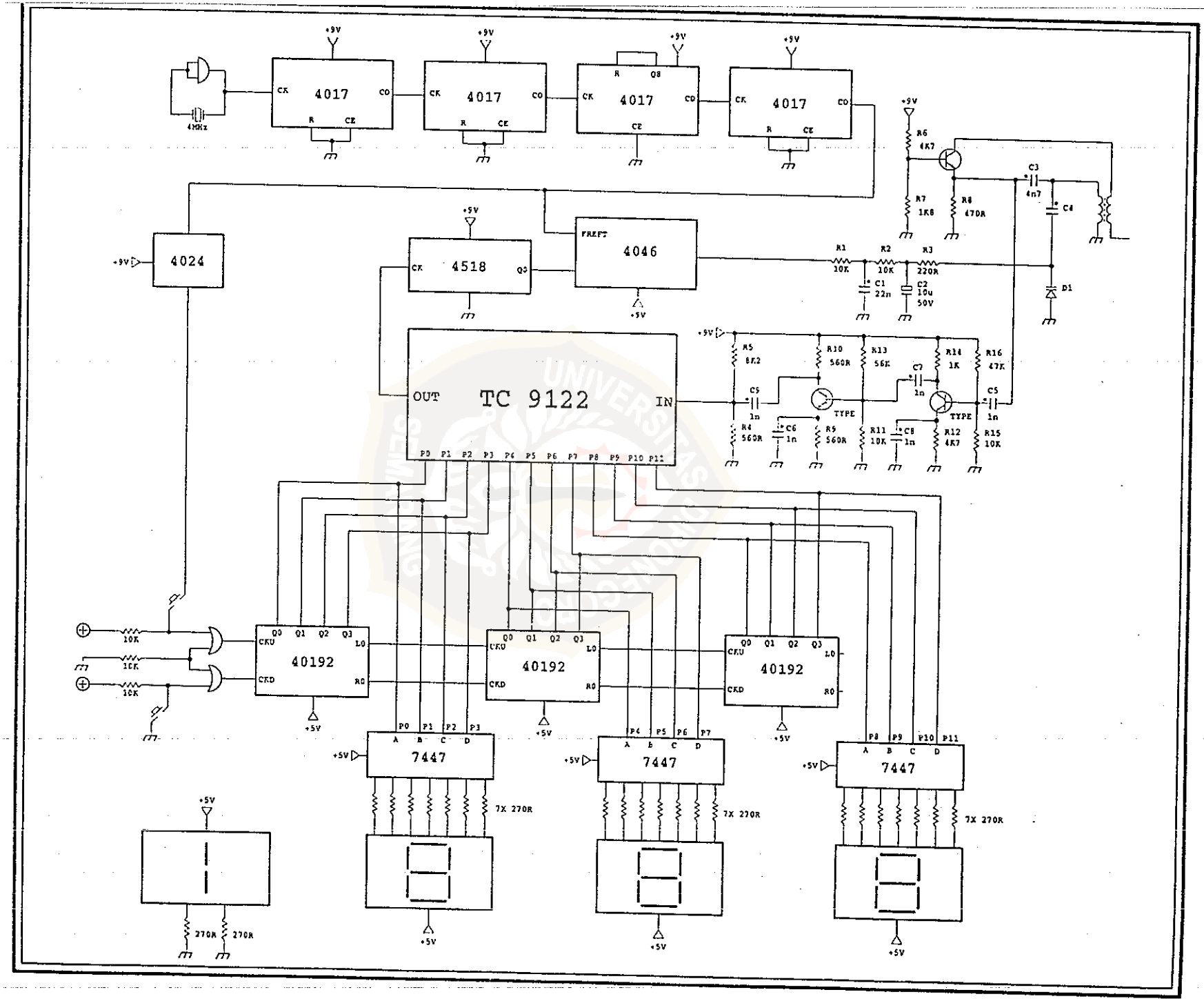


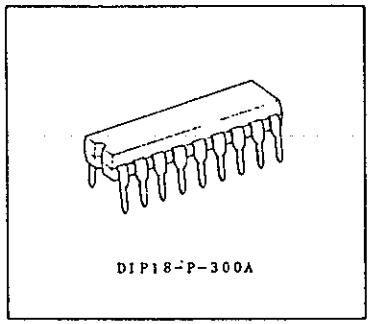
TC9122P HIGH-SPEED BCD PROGRAMMABLE COUNTER

TC9122P is high-speed programmable counter of C-MOS structure developed for PLL circuits and various frequency dividers, and is provided with the following features.

- Permits epoch-making high-speed operation for C-MOS structure.

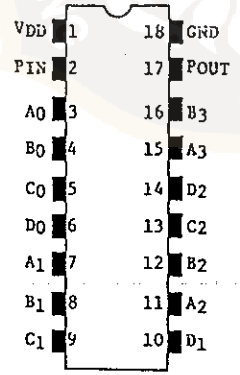
  f_{max} = 15MHz (V_{DD}=7.5V, Ta=-30 ∿ 75°C, V_{IN}=2.0Vp-p)

- Program data are input by means of BCD code, allowing frequency division of 8 ∿ 3999.
- Built-in self-bias type amplifier for divided frequency signal input is capable of operation by small signal in combination with capacitor.
- C-MOS structure provides wide range of operational supply voltage (4.5 ∿ 8.5V) and simplification of design.



Weight : 1.4g(Typ.)

PIN CONNECTION

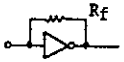
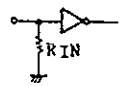


(TOP VIEW)

MAXIMUM RATINGS (Ta=25°C)

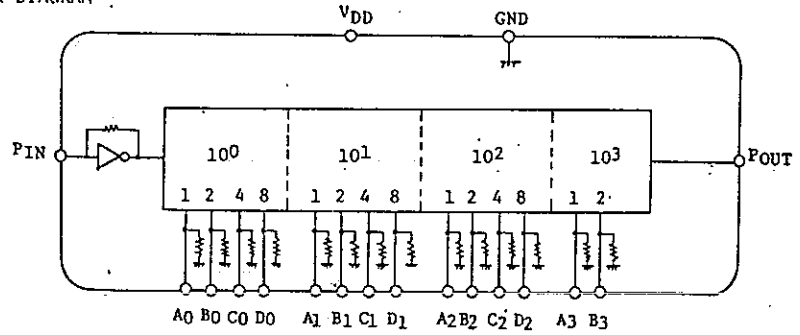
CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	-0.3 ∿ 10	V
Input Voltage	V_{IN}	-0.3∿V_{DD}+0.3	V
Operating Temp.	Topr	-30 ∿ 75	°C
Storage Temperature	Tstg	-55 ∿ 125	°C

FUNCTIONAL DESCRIPTION OF EACH TERMINAL

PIN NO.	SYMBOL	NAME	FUNCTIONAL DESCRIPTION	REMARKS
2	P_{IN}	Programmable counter input terminal	Divided frequency signal input terminal of programmable counter. Built-in self-bias amplifier is capable of operation by small signal in combination with capacitor.	Built-in amplifier 
3∿16	A_0 ∿ D_0 ×10^0 A_1 ∿ D_2 ×10^1 A_2 ∿ D_2 ×10^2 A_3, B_3 ×10^3	Program input terminal	Input terminals to establish frequency division ratio N by BCD. Program data allow frequency division of 8∿3999 by $3\frac{1}{2}$-digit BCD. The following frequency division ratio combinatios are inhibited.	Pull/down resistor contained in each terminal. 
17	P_{OUT}	Programmable counter output terminal	Output terminal of programmable counter. This terminal is for 1/N frequency output of P_{IN} input frequency. Pulse width is for 5 bits of input.	
1,18	V_{DD} GND		Terminal to which supply voltage is applied.	

A_0	B_0	C_0	D_0	A_1	B_1	C_1	D_1	A_2	B_2	C_2	D_2	A_3	A_3
1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (Unless otherwise specified Ta=25°C, V_{DD}=7.5V)

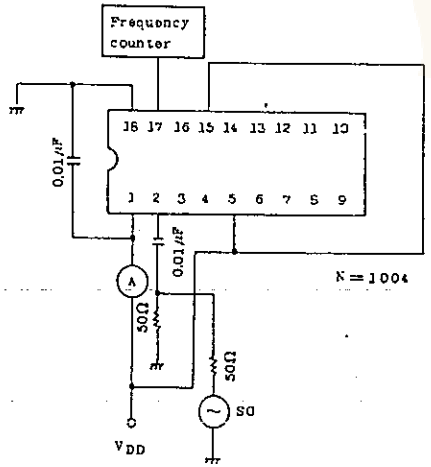
CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage		V_{DD}	-	-	4.5	~	8.5	V
Operating Input Amplitude		V_{IN}	-	-	2.0	~	7.0	V_{p-p}
Operating Supply Current		I_{DD}	1	f_{IN}=15MHz, V_{IN}=2.0Vp-p	-	15	30	mA
Input Voltage	"H" Level	V_{IH}	-	-	5.5	-	-	V
	"L" Level	V_{IL}	-	-	-	-	2.0	V
Output Voltage	"H" Level	V_{OH}	-	I_{OH}=-0.5mA	6.5	-	-	V
	"L" Level	V_{OL}	-	I_{OL}=0.5mA	-	-	1.0	V
Operating Frequency Range		fopr	1	(Note 1)	1	~	15	MHz
Input Pull Down Resistance		R_{IN}	-	-	20	-	80	kΩ
Amp. Feedback Resistance		Rf	-	-	100	-	500	kΩ

(Note 1) This operational frequency satisfies the specification during the following conditions.

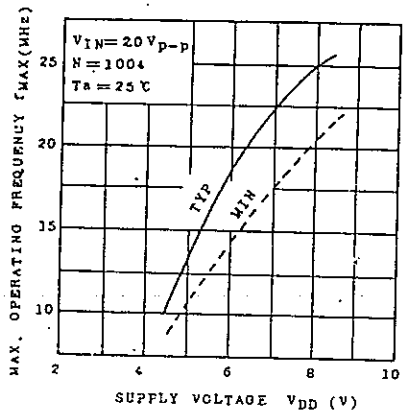
V_{DD} = 7.5V ± 10%, V_{IN} = 2.0Vp-p, Ta = -30 ~ 75°C

TEST CIRCUIT 1

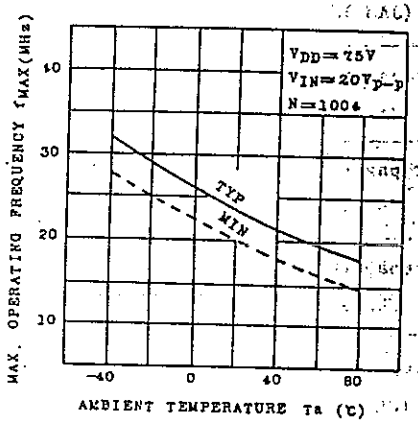
I_{DD}, fopr



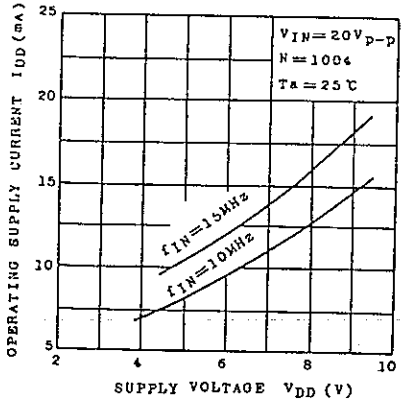
V_{DD} - f_{MAX}



Ta - f_{MAX}



V_{DD} - I_{DD}

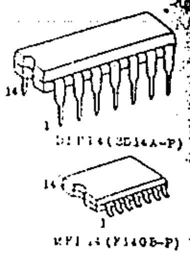


TC4024BP/BF

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4024BP/TC4024BF 7 STAGE RIPPLE-CARRY BINARY COUNTER/DIVIDERS

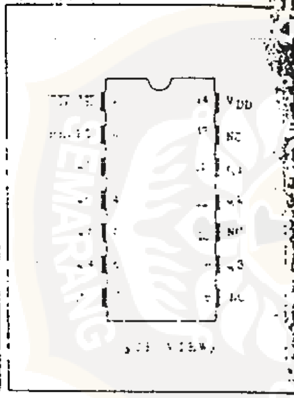
TC4024BP/BF is 7 stage ripple carry type binary counter having asynchronous clear function.
The counter advances its counting state by falling edge of $\overline{CLOCK}$ input.
When RESET input is placed at "H", all the internal flip-flops are reset making all the outputs Q1 through Q7 to be "L" regardless of $\overline{CLOCK}$ input.
This is suitable for frequency divider circuits and control circuits.



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS} - 0.5 ~ V_{SS} + 20	V
Input Voltage	V_{IN}	V_{SS} - 0.5 ~ V_{DD} + 0.5	V
Output Voltage	V_{OUT}	V_{SS} - 0.5 ~ V_{DD} + 0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(SEP)	mW
Operating Temperature Range	T_{opr}	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT

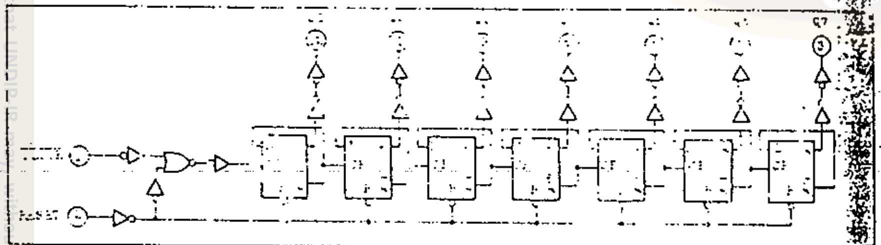


TRUTH TABLE

[illegible]	[illegible]	[illegible]
[illegible]	H	[illegible]
[illegible]	[illegible]	No Change
[illegible]	[illegible]	[illegible]

[illegible]

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNITS
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

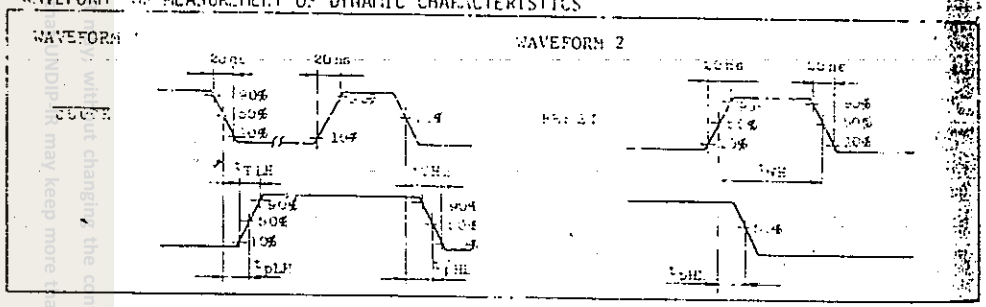
CHARACTERISTIC	SYMBOL	TEST CONDITIONS	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNITS
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|$<1μA, V_{IN}=V_{SS}, V_{DD}	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|$<1μA, V_{IN}=V_{SS}, V_{DD}	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.2	-	-0.16		-	-0.12	-	mA
		V_{OH}=2.5V	5	-	-	-		-	-	-	
		V_{OH}=9.5V	10	-0.5	-	-0.4		-	-0.3	-	
		V_{OH}=13.5V, V_{IN}=V_{SS}, V_{DD}	15	-1.4	-	-1.2		-	-1.0	-	
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.52	-	0.44		-	0.36	-	
		V_{OL}=0.5V	10	1.3	-	1.1		-	0.9	-	
		V_{OL}=1.5V, V_{IN}=V_{SS}, V_{DD}	15	3.6	-	3.0		-	2.4	-	
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V, 13.5V, $\|I_{OUT}\|$<1μA	15	11.0	-	11.0	8.25	-	11.0	-	
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0		3.0	
		V_{OUT}=1.5V, 13.5V, $\|I_{OUT}\|$<1μA	15	-	4.0	-	6.75	4.0	-	4.0	
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.3	-	10^{-5}	0.3	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	
Quiescent Device Current	I_{DD}	V_{IN}=V_{SS}, V_{DD} *	5	-	20	-	0.005	20	-	150	μA
			10	-	40	-	0.010	40	-	300	
			15	-	80	-	0.015	80	-	600	

* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	
Output Transition Time (Low to High)	t_{TLH}		5	–	100	200	ns
			10	–	50	100	
			15	–	40	80	
Output Transition Time (High to Low)	t_{THL}		5	–	100	200	ns
			10	–	50	100	
			15	–	40	80	
Propagation Delay Time (CLOCK - Q1)	t_{pLH}		5	–	180	360	ns
			10	–	80	160	
			15	–	65	130	
Propagation Delay Time (CLOCK - Q1)	t_{pHL}		5	–	180	360	ns
			10	–	80	160	
			15	–	65	130	
Propagation Delay Time (CLOCK - Q7)	t_{pLH}		5	–	600	1200	ns
			10	–	260	520	
			15	–	215	430	
Propagation Delay Time (CLOCK - Q7)	t_{pHL}		5	–	600	1200	ns
			10	–	260	520	
			15	–	215	430	
Propagation Delay Time (RESET - Q)	t_{pHL}		5	–	140	280	ns
			10	–	60	120	
			15	–	50	100	
Max. Clock Frequency	f_{CL}		5	3.5	8	–	MHz
			10	8	20	–	
			15	12	25	–	
Max. Clock Input Rise Time	t_{rCL}		5	20	–	–	μs
Max. Clock Input Fall Time	t_{fCL}		10	2.5	–	–	
			15	1.5	–	–	
Min. Pulse Width (RESET)	t_{WH}		5	–	100	200	ns
			10	–	40	80	
			15	–	30	60	
Input Capacitance	C_{IN}			–	5	7.5	pF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS



TC4027BP/BF

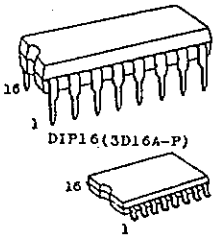
TC4027BP/TC4027BF DUAL J-K MASTER-SLAVE FLIP-FLOP

TC4027BP/BF is J-K master-slave flip-flop having RESET and SET functions.

In the case of J-K mode, when the clock input is given with both RESET and SET at "L", the output changes at rising edge of the clock according to the states of J and K.

When RESET is placed at "H", output Q becomes "L" regardless of other inputs and when SET is placed at "H" and RESET at "L", Q becomes "H" regardless of other inputs. (R-S mode)

When both of RESET and SET are at "H", takes precedence resulting Q="L" and Q="H".



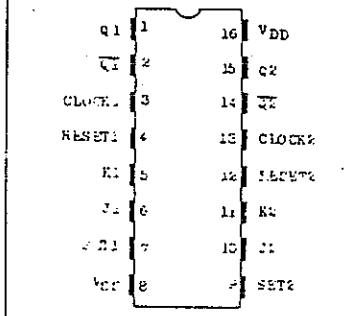
DIP16(3D16A-P)

MFP16(F160C-P)

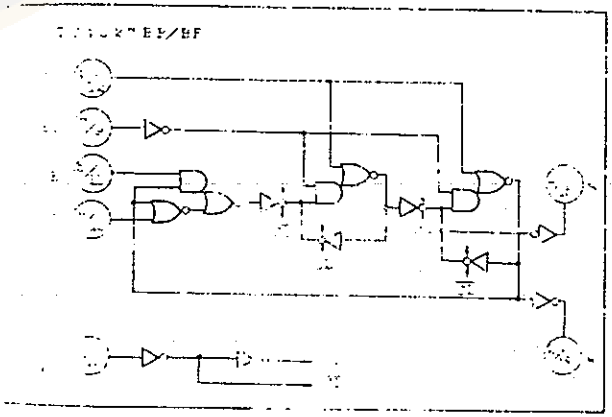
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS} - 0.5 ~ V_{SS} + 20	V
Input Voltage	V_{IN}	V_{SS} - 0.5 ~ V_{DD} + 0.5	V
Output Voltage	V_{OUT}	V_{SS} - 0.5 ~ V_{DD} + 0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

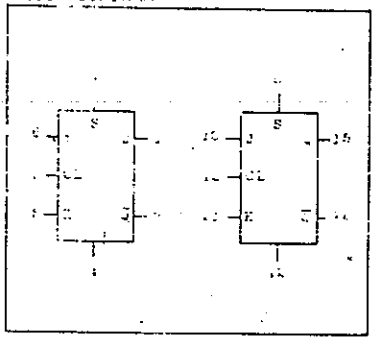
PIN ASSIGNMENT



LOGIC DIAGRAM

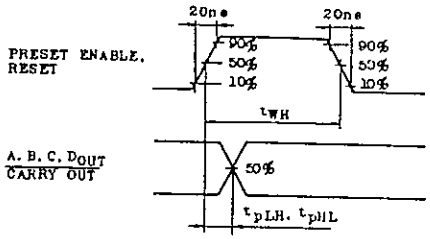


CLOCK DIAGRAM

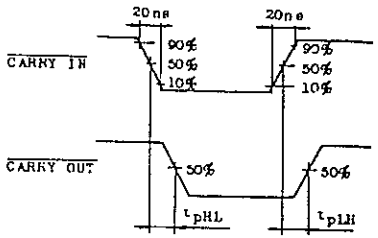


WAVEFORMS FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

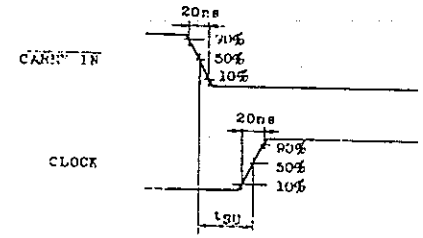
WAVEFORM 2



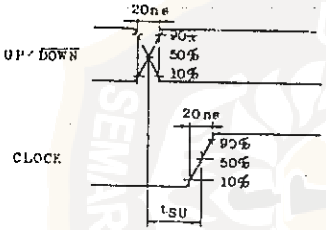
WAVEFORM 3



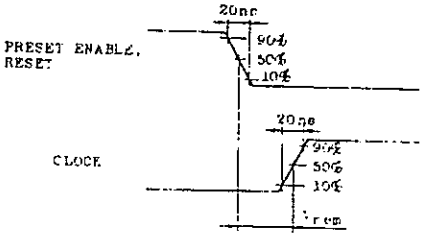
WAVEFORM 4



WAVEFORM 5

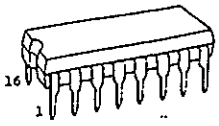


WAVEFORM 6

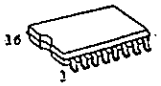


TC4518BP/TC4518BF DUAL BCD UP COUNTER
TC4520BP/TC4520BF DUAL BINARY UP COUNTER

TC4518BP/BF and TC4520BP/BF are up counters of BCD or 4 bit binary.
Since both of TC4518BP/BF and TC4520BP/BF contain two independent circuits of counters with the same functions in one package, counting or frequency division of two BCD digits or eight binary bits can be achieved with one IC. The counters can be reset to "0" (Q0 ~ Q3="L") by giving "H" level signal to RESET input regardless of other inputs.
The counting condition is changed by the rising edge of CLOCK input if ENABLE="H" or by the falling edge of ENABLE if CLOCK="L".



DIP16 (3D16A-P)

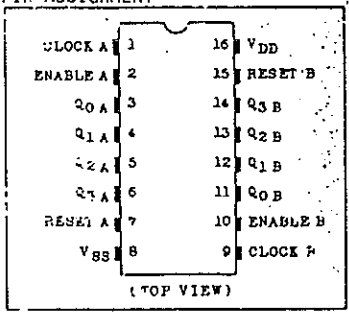


MFP16 (F16GC-P)

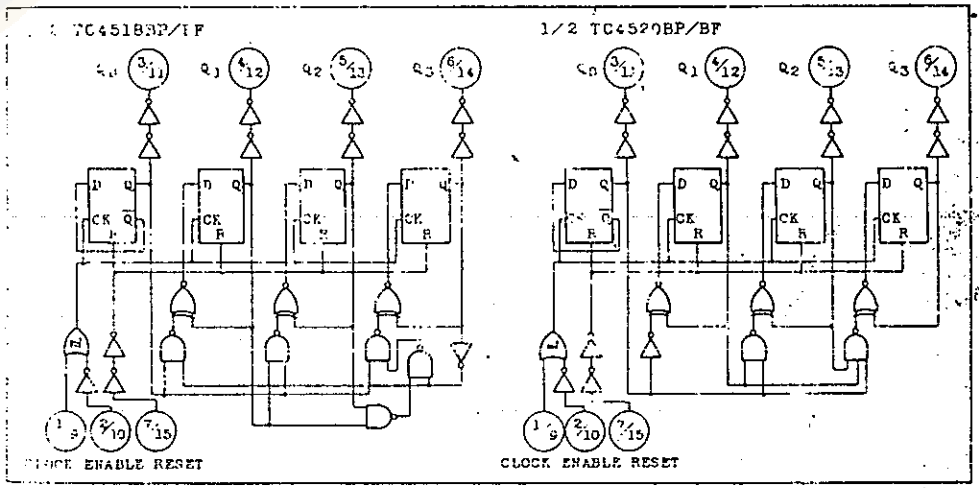
ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10sec	

PIN ASSIGNMENT

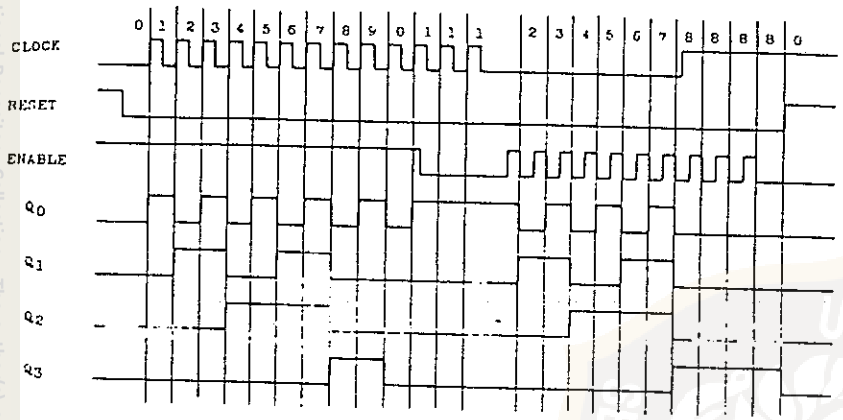


LOGIC DIAGRAM

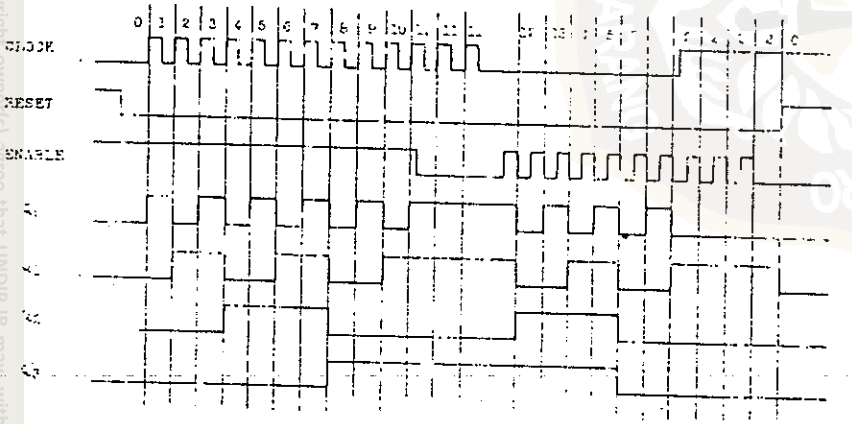


TIMING CHART

TC4518BP/BF



TC4520BP/BF



RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0		V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

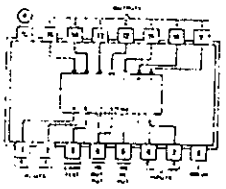
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	4.95	-	4.95	5.00	-	4.95	-	V
			10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|<1\mu A$ $V_{IN}=V_{SS},V_{DD}$	5	-	0.05	-	0.00	0.05	-	0.05	
			10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.05	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|<1\mu A$									
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|<1\mu A$									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	
Quiescent Device Current	I_{DD}	$V_{IN}=V_{SS},V_{DD}$ *	5	-	5	-	0.005	5	-	150	μA
			10	-	10	-	0.010	10	-	300	
			15	-	20	-	0.015	20	-	600	

* All valid input combinations.

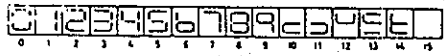
46, 246 Penggerak/dekoder BCD-7-segmen dengan jalankeluar kolektor terbuka (30 V)

47, 247 dengan jalankeluar kolektor terbuka (15 V)

347, 447 dengan jalankeluar kolektor terbuka (7 V)



SEGMENT IDENTIFICATION



NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS (6= 6 and 9= 9 for 246, 247, LS247 and LS447)

Decimal or function	Inputs LT	RBI	D	C	B	A	BI/RBO†	Outputs a	b	c	d	e	f	g	note
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	OFF	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	1
9	H	X	H	L	L	H	H	ON	ON	ON	ON	OFF	ON	ON	
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	4

Function table
- ○ 46A, 47A, LS47, LS347
- ● 246, 247, LS247, LS447

CATATAN:

1. Jalanmasuk polosan ($\overline{BI}$) harus terbuka atau ditaruh pada taraf logika tinggi bila fungsi-fungsi keluaran 0 hingga 15 diinginkan. Jalanmasuk polosan deret ($\overline{RBI}$) harus terbuka atau tinggi kalau pemolosan nol dasan tidak diinginkan.
2. Kalau taraf logika rendah dikenakan dengan langsung kepada jalanmasuk polosan ($\overline{BI}$), maka semua jalankeluar segmen adalah off tak perduli akan taraf yang ada di sebarang jalanmasuk lain.
3. Bila jalanmasuk polosan deret ($\overline{RBI}$) dan juga jalanmasuk-jalanmasuk A, B, C, dan D berada dalam taraf rendah dengan *lamp test* tinggi, maka semua segmen keluaran off dan jalankeluar polosan deret ($\overline{RBO}$) pergi ke taraf rendah (kondisi tanggap).
4. Kalau jalanmasuk polosan/jalankeluar polosan deret ($\overline{BI}/\overline{RBO}$) terbuka atau dibiarkan tinggi, dan jalanmasuk *lamp test* dibuat rendah, maka semua segmen keluaran adalah on.

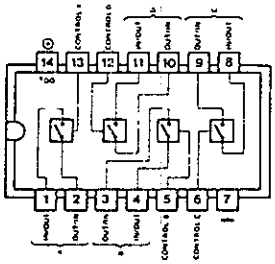
† $\overline{BI}/\overline{RBO}$ adalah logika AND kawat yang berguna sebagai jalanmasuk polosan ($\overline{BI}$) dan/atau jalankeluar polosan deret ($\overline{RBO}$)

	supply curr. (mA)	t_{PLH} (ns)	t_{PHL} (ns)
46A 47A 246 247	64	100	100
LS47 LS247 LS347 LS447	7	100	100

		Condition	Fan-in	Fan-out
46A 47A	$\overline{BI}/\overline{RBO}$ inp.	L	2,5	
		H	1	
246 247	other inp.	L/H	1	
	$\overline{BI}/\overline{RBO}$ outp.	L/H		5
	other outp.	L		25
LS47 LS247	$\overline{BI}/\overline{RBO}$ inp.	L	3	
		H	1	
	other inp.	L/H	1	
	$\overline{BI}/\overline{RBO}$ outp.	L		8
		H		2,5
	other outp.	L		60
LS347 LS447	$\overline{BI}/\overline{RBO}$ inp.	L	3	
		H	1	
	other inp.	L/H	1	
	$\overline{BI}/\overline{RBO}$ outp.	L		8
		H		2,5
	other outp.	L		60

IC CMOS

4016–4017



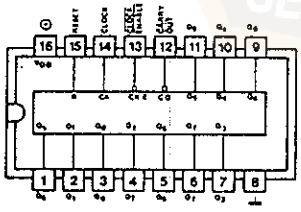
4016 SAKLAR DUASISI (BILATERAL), BEREMPAT
4066 SAKLAR DUASISI (BILATERAL), BEREMPAT

4016, 4066 terdiri atas empat saklar mandiri yang mampu mengendalikan isyarat digit atau isyarat analog. TINGGI pada jalanmasuk kemudi mengadakan jalanan dua-arah berimpedansi rendah antara *In/Out* dan *Out/In* (kondisi *ON*).
RENDAH pada jalanmasuk kemudi melumpuhkan saklar-saklar; impedansi tinggi antara *In/Out* dan *Out/In* (kondisi *OFF*).
Pada penerapan tertentu, arus yang ada pada resistor beban (R_L) mungkin mencakup komponen V_{DD} dan saluran isyarat. Guna mencegah mengalirnya arus V_{DD} selama arus saklar mengalir ke terminal-terminal 1, 4, 8 atau 11, maka perosotan tegangan di antara saklar dua-arah tidak boleh melampaui 0,3 V. Tidak akan ada arus V_{DD} mengalir pada R_L kalau arus saklar mengalir ke terminal 2, 3, 9 atau 10.

Karakteristik elektrik (Motorola) T = 250° C

		4016			4066			
(Typ.)	V_{DD}	5	10	15	5	10	15	V
"ON" Resistance		300	260	260	250	120	80	Ω
Δ "ON" resistance between any two circuits in a common package		15			25	10	5	Ω
Crosstalk between any two switches $20 \log \frac{V_{out(B)}}{V_{in(A)}} = -50$ dB			1.25			8		MHz
Frequency response (−3 dB)			40			65		MHz
Max. Control input pulse frequency		5	10	12	6	8	8.5	MHz
Crosstalk Control input to signal output		30	50	100		300		mV
Sine wave distortion			0.16			0.1		%
Input current control			10			10		nA

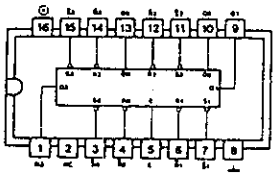
		Conditions
"ON" Resistance		R_L = 10 kΩ
Δ "ON" resistance between any two circuits in a common package		
Crosstalk between any two switches $20 \log \frac{V_{out(B)}}{V_{in(A)}} = -50$ dB		R_L = 1 kΩ Switch A ON Switch B OFF
Frequency response (−3 dB)		R_L = 1 kΩ Switch ON
Max. Control input pulse frequency		R_L = 1 kΩ
Crosstalk Control input to signal output		f = 1 kHz
Sine wave distortion		R_L = 10 kΩ f = 1 kHz
Input current control		



4017 PEMBAGI/PENCACAH DEKADA DENGAN 10 JALANKELUAR TERBACA SANDINYA *(DECODED)*
Pencacah dimulaikan dengan transisi RENDAH ke TINGGI pada jalanmasuk lonceng (CK) sementara jalanmasuk $\overline{CKE}$ sedang RENDAH, ataupun dimulaikan dengan transisi TINGGI ke RENDAH pada jalanmasuk $\overline{CKE}$ sementara jalanmasuk lonceng CK adalah TINGGI.
Kalau pencacah-pencacah 4017 dikaskadakan, jalankeluar *Carry Out* akan dapat dipakai untuk menggerakkan jalanmasuk lonceng 4017 berikutnya. Jalankeluar *Carry Out* tersebut sedang

IC CMOS

4044...4046

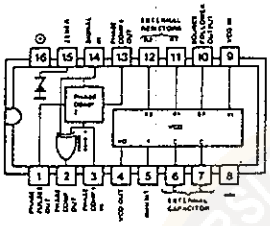


4044 GERENDEL R-S 'NAND' DENGAN JALANKELUAR 3-STATUS, BEREMPAT

4044 adalah sebuah gerendel RS dengan jalankeluar-jalankeluar 3-status, dengan satu jalankeluar *Enable* (E) yang dipakai bersama. Tiap gerendel memiliki jalanmasuk *Set* (S) aktif RENDAH, sebuah jalanmasuk *Reset* (R) aktif RENDAH dan sebuah jalankeluar (Q) 3-status aktif TINGGI.

Tabel benaran

S	R	E	Q
X	X	0	High Impedance
0	0	1	*
0	1	1	1
1	0	1	0
1	1	1	No change



4046 IKAL TERKUNCI-FASA *(Phase-Locked Loop)* DAYA MIKRO

Ikal terkunci fasa *(PLL)* 4046 terdiri atas dua penanding fasa, sebuah osilator terkemudi-fasa *(voltage-controlled oscillator, VCO)*, pengikut sumber, dan dioda zener. Penanding memiliki dua jalanmasuk isyarat yang dipakai bersama *(common), Signal In* dan *Phase Comp. In*. Jalanmasuk *Signal In* dapat dipakai dengan dikopelkan secara langsung kepada isyarat-isyarat tegangan tinggi, ataupun terkopel secara tak langsung (dengan kondensator deretan) kepada isyarat-isyarat tegangan rendah.

Rangkaian panjaranan-diri *(selfbias)* menepatkan isyarat tegangan rendah pada daerah linier penguatnya. Penanding fasa 1 (sebuah gerbang EXOR) menyediakan isyarat keliru berdigit di jalankeluar *Phase Comp 1 Out*, dan mempertahankan selisih fasa 90° C di frekuensi senter antara isyarat-isyarat *Signal In* dan *Phase Comp In* (kedua-duanya pada 50% daur aktif). Penanding fasa 2 (dengan logika pengindera tepian depan) menyediakan isyarat-isyarat keliru untuk jalankeluar *Phase Comp 2 Out* dan *Phase Pulses Out*, dan mempertahankan selisih fasa 0° C antara isyarat-isyarat *Signal In* dan *Phase Comp In* (tak menghiraukan daur aktif). VCO yang linier mengeluarkan isyarat keluaran *VCO Out* yang frekuensinya ditentukan oleh tegangan di jalanmasuk *VCO In* dan kondensator serta resistor yang dikoneksikan pada penc-pena pengindera

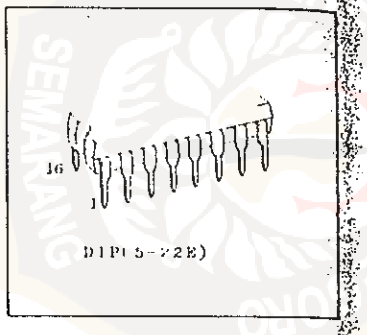
TC74HC192P SYNCHRONOUS UP/DOWN DECADE COUNTER
TC74HC193P SYNCHRONOUS UP/DOWN BINARY COUNTER

GENERAL DESCRIPTION

The TC74HC192 and TC74HC193 are high speed CMOS SYNCHRONOUS 4-BIT UP/DOWN COUNTER fabricated with silicon gate C^2MOS technology. They achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipaiton. These counters have a clear input(CLEAR), a load input($\overline{LOAD}$), load data inputs(A - D), two clock inputs(COUNT UP/COUNT DOWN), four count data outputs(Q_A - Q_D) and carry and borrow outputs. CLEAR is active high and forces Q_A thru Q_D outputs low independently of the other inputs. $\overline{LOAD}$ is active low and load the load data when CLEAR input is held low. COUNT UP input pulse and COUNT DOWN input pulse independently bring a up-counting or down at the positive going transition of each clock pulse. CARRY and BORROW outputs are provided in order to make a cascade connection without external circuitry. All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ..... f_{MAX}=32MHZ(Typ.) at V_{CC}=5V
- Low Power Dissipation ..... I_{CC}=4μA(Max.) at Ta=25°C
- High Noise Immunity ..... $V_{NIH}=V_{NIL}$=28% V_{CC}(Min.)
- Output Drive Capability ..... 10 LSTTL Loads
- Symmetrical Output Impedance .....$|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ..... $t_{pLH}=t_{pHL}$
- Wide Operating Voltage Range ..... $V_{CC(opr.)}$=2V ~ 6V
- Pin and Function Compatible with 74LS192/193

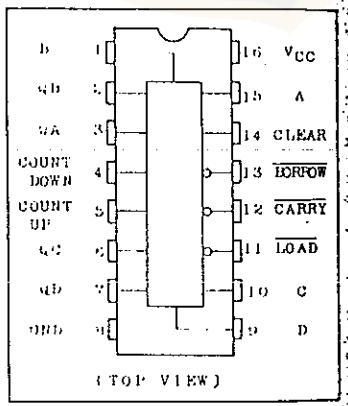


ABSOLUTE MAXIMUM RATINGS

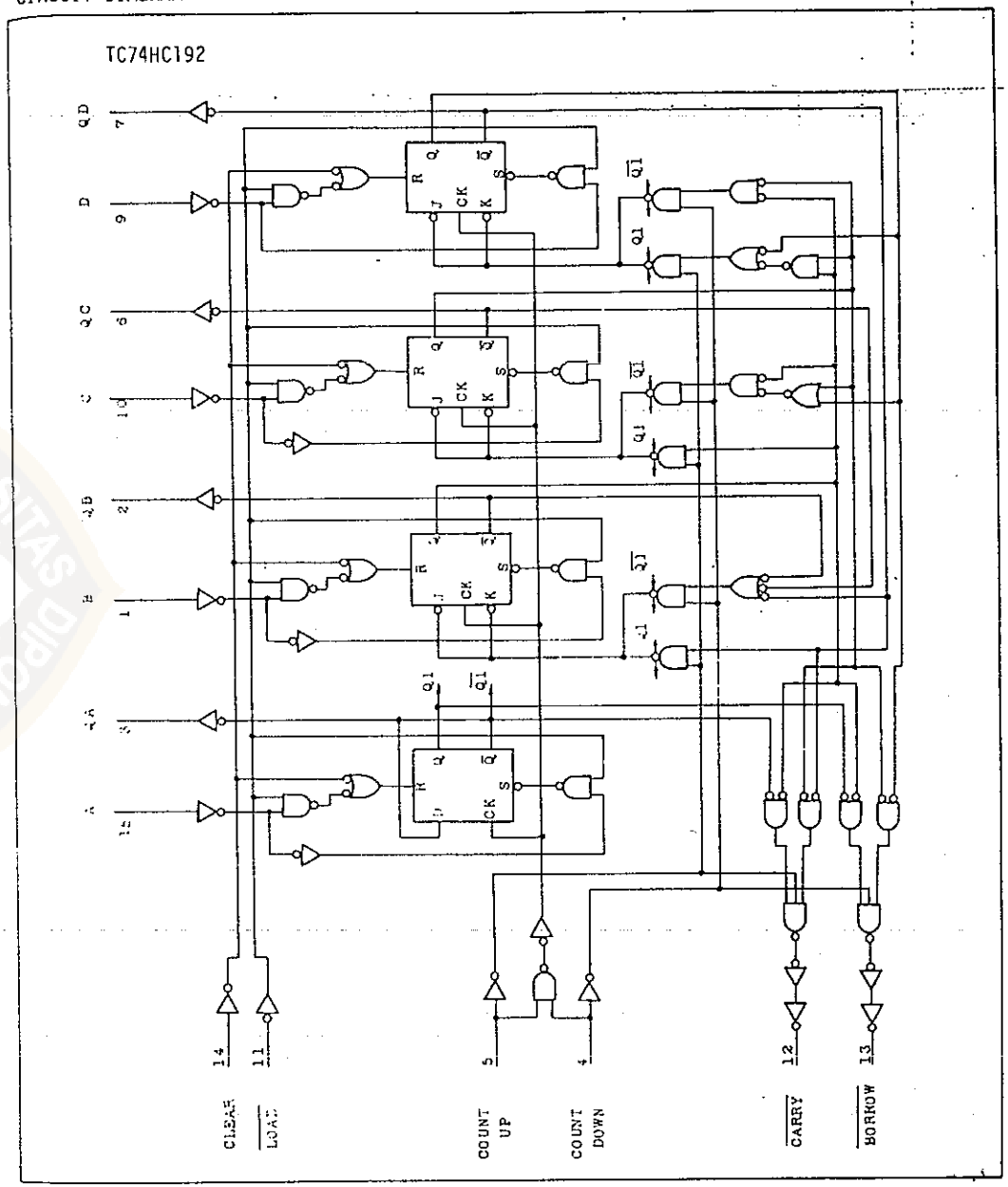
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC}+0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC}+0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500*	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

* 500mW in the range of Ta=-40° ~ 65°C and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

PIN ASSIGNMENT

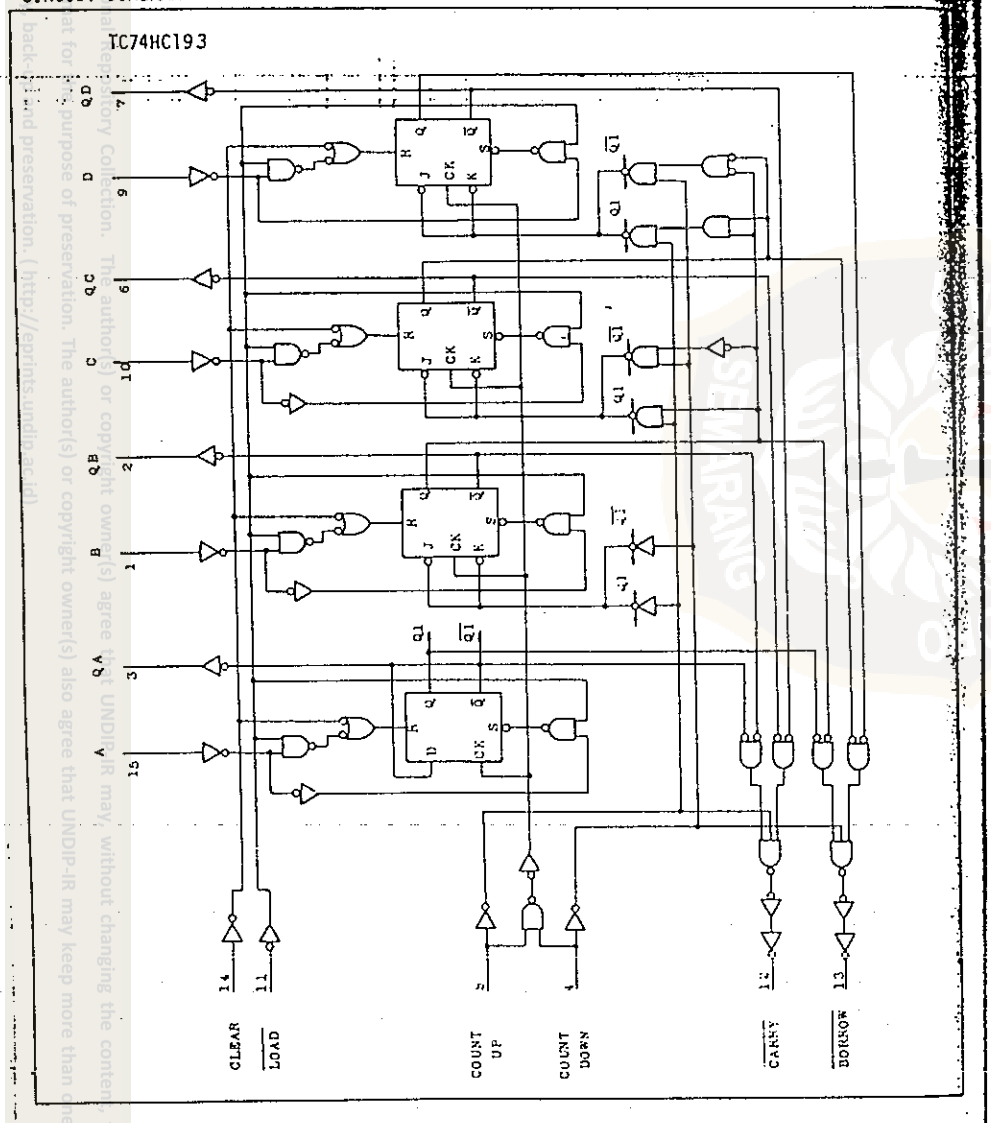


CIRCUIT DIAGRAM

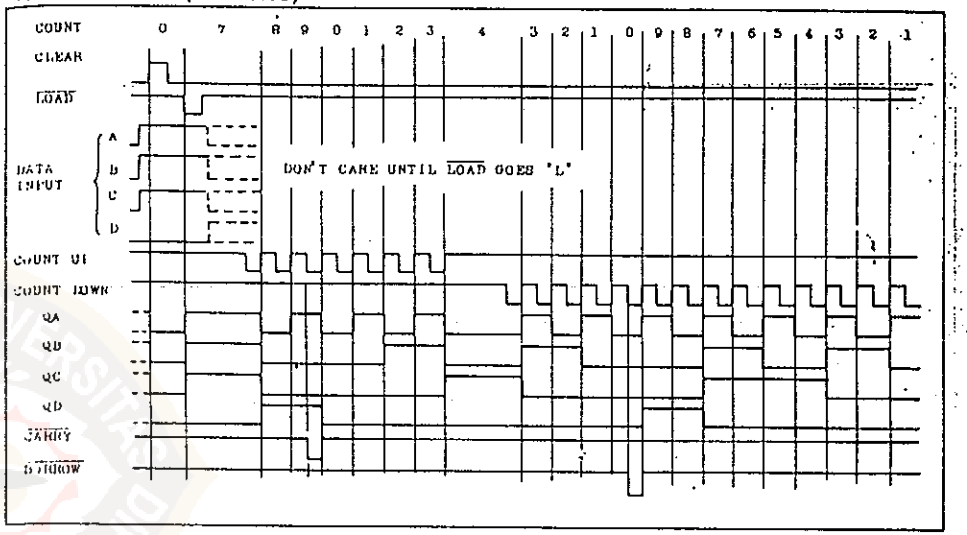


CIRCUIT DIAGRAM

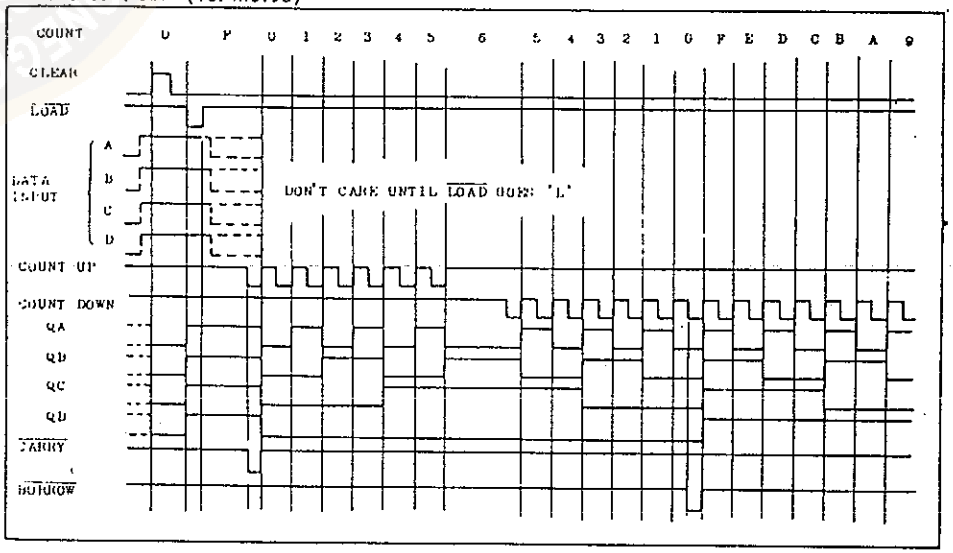
TC74HC193



TIMING DIAGRAM (TC74HC192)



TIMING DIAGRAM (TC74HC193)



TRUTH TABLE

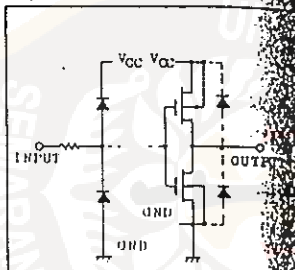
COUNT UP	COUNT DOWN	$\overline{LOAD}$	CLEAR	FUNCTION
⌐¬	H	H	L	COUNT UP
¬⌐	H	H	L	NO COUNT
H	⌐¬	H	L	COUNT DOWN
H	¬⌐	H	L	NO COUNT
X	X	L	L	PRESET
X	X	X	H	RESET

X : DON'T CARE

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 1000 (V_{CC}=2.0V) 0 ~ 500 (V_{CC}=4.5V) 0 ~ 400 (V_{CC}=6.0V)	ns

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	TYP.	MAX.	Ta=−40~85°C MIN.	MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	–	–	1.5	–	V
				4.5	3.15	–	–	3.15	–	
				6.0	4.2	–	–	4.2	–	
Low-Level Input Voltage	V_{IL}			2.0	–	–	0.5	–	0.5	V
				4.5	–	–	1.35	–	1.35	
				6.0	–	–	1.8	–	1.8	
High-Level Output Voltage	V_{OH}	V_{IN}=V_{IH} or V_{IL}	I_{OH}=−20μA	2.0	1.9	2.0	–	1.9	–	V
				4.5	4.4	4.5	–	4.4	–	
				6.0	5.9	6.0	–	5.9	–	
			I_{OH}=−4mA	4.5	4.18	4.31	–	4.13	–	
			I_{OH}=−5.2mA	6.0	5.68	5.80	–	5.63	–	

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25°C MIN.	TYP.	MAX.	Ta=−40~85°C MIN.	MAX.	UNIT
Low-Level Output Voltage	V_{OL}	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0	–	0.0	0.1	–	0.1	V
				4.5	–	0.0	0.1	–	0.1	
				6.0	–	0.0	0.1	–	0.1	
			I_{OL}=4mA	4.5	–	0.17	0.32	–	0.37	
			I_{OL}=5.2mA	6.0	–	0.18	0.32	–	0.37	
Input Leakage Current	I_{IN}	V_{IN}=V_{CC} or GND		6.0	–	–	±0.1	–	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN}=V_{CC} or GND		6.0	–	–	4.0	–	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, INPUT t_r=t_f=6nS)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	TYP.	MAX.	Ta=−40~85°C MIN.	MAX.	UNIT
Output Transition Time	t_{TLH}		2.0	–	30	75	–	90	ns
	t_{THL}		4.5	–	8	15	–	18	
			6.0	–	7	13	–	16	
Propagation Delay Time (UP, DOWN − Q)	t_{PLH}		2.0	–	100	205	–	250	
	t_{PHL}		4.5	–	26	41	–	50	
			6.0	–	22	35	–	43	
Propagation Delay Time ($UP - \overline{CARRY}$)	t_{PLH}		2.0	–	75	160	–	195	
	t_{PHL}		4.5	–	20	32	–	39	
			6.0	–	17	28	–	34	
Propagation Delay Time (DOWN − $\overline{BORROW}$)	t_{PLH}		2.0	–	75	160	–	195	
	t_{PHL}		4.5	–	20	32	–	39	
			6.0	–	17	28	–	34	
Propagation Delay Time ($\overline{LOAD}$ − Q)	t_{PLH}		2.0	–	125	270	–	325	
	t_{PHL}		4.5	–	35	54	–	65	
			6.0	–	30	46	–	56	
Propagation Delay Time ($\overline{LOAD}$ − $\overline{CARRY}$)	t_{PLH}		2.0	–	180	345	–	415	
	t_{PHL}		4.5	–	45	69	–	83	
			6.0	–	39	59	–	56	
Propagation Delay Time ($\overline{LOAD}$ − $\overline{BORROW}$)	t_{PLH}		2.0	–	165	310	–	375	
	t_{PHL}		4.5	–	40	62	–	75	
			6.0	–	34	53	–	64	

AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Propagation Delay Time (JAM IN - Q)	t_{PLH} t_{PHL}		2.0	-	120	250	-	300	ns
			4.5	-	32	50	-	60	
			6.0	-	28	43	-	51	
Propagation Delay Time (JAM IN - $\overline{CARRY}$)	t_{PLH} t_{PHL}		2.0	-	170	330	-	400	
			4.5	-	43	66	-	80	
			6.0	-	37	57	-	68	
Propagation Delay Time (JAM IN - $\overline{BORROW}$)	t_{PLH} t_{PHL}		2.0	-	165	310	-	345	
			4.5	-	40	62	-	69	
			6.0	-	33	49	-	59	
Propagation Delay Time (CLEAR - Q)	t_{PHL}		2.0	-	135	270	-	325	
			4.5	-	35	54	-	65	
			6.0	-	30	46	-	56	
Propagation Delay Time (CLEAR - $\overline{CARRY}$)	t_{PLH}		2.0	-	160	310	-	375	
			4.5	-	40	62	-	75	
			6.0	-	34	53	-	64	
Propagation Delay Time (CLEAR - $\overline{BORROW}$)	t_{PHL}		2.0	-	160	310	-	375	
			4.5	-	40	62	-	75	
			6.0	-	34	53	-	64	
Maximum Frequency (CLOCK)	f_{MAX}		2.0	3	6	-	2.5	-	MHz
			4.5	15	30	-	12	-	
			6.0	17	35	-	14	-	
Minimum Pulse Width (CLOCK)	$t_{w(H)}$ $t_{w(L)}$		2.0	-	90	150	-	180	ns
			4.5	-	18	30	-	36	
			6.0	-	16	26	-	31	
Minimum Pulse Width ($\overline{LOAD}$)	$t_{w(H)}$		2.0	-	50	100	-	120	
			4.5	-	12	20	-	24	
			6.0	-	11	17	-	21	
Minimum Pulse Width (CLEAR)	$t_{w(H)}$		2.0	-	50	125	-	150	
			4.5	-	13	25	-	30	
			6.0	-	11	22	-	26	
Minimum Removal Time ($\overline{LOAD}$)	t_{rem}		2.0	-	22	75	-	90	
			4.5	-	5	15	-	18	
			6.0	-	5	13	-	16	
Minimum Removal Time (CLEAR)	t_{rem}		2.0	-	10	50	-	60	
			4.5	-	1	10	-	12	
			6.0	-	1	9	-	11	

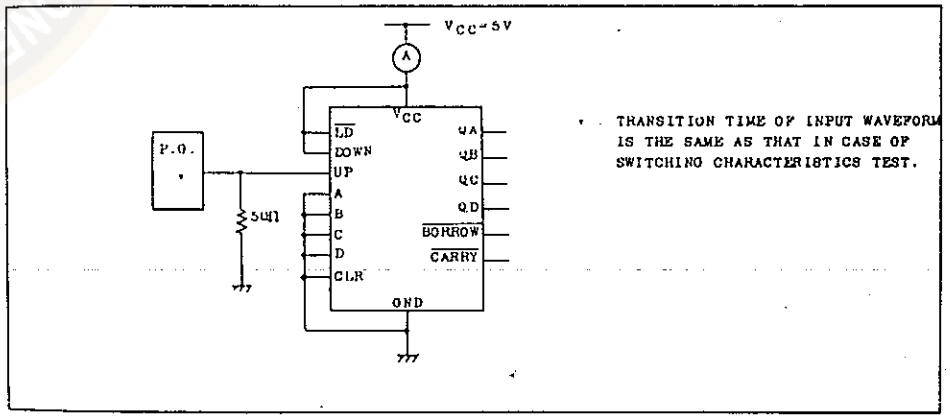
AC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC}	Ta=25°C MIN.	Ta=25°C TYP.	Ta=25°C MAX.	Ta=-40~85°C MIN.	Ta=-40~85°C MAX.	UNIT
Minimum Set-up Time (DATA - $\overline{LOAD}$)	t_s		2.0	-	55	100	-	120	ns
			4.5	-	11	20	-	24	
			6.0	-	10	17	-	21	
Minimum Hold Time (DATA - $\overline{LOAD}$)	t_h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Input Capacitance	C_{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C_{PD}(1)			-	66	-	-	-	

Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit). Average operating current can be obtained by the equation hereunder.

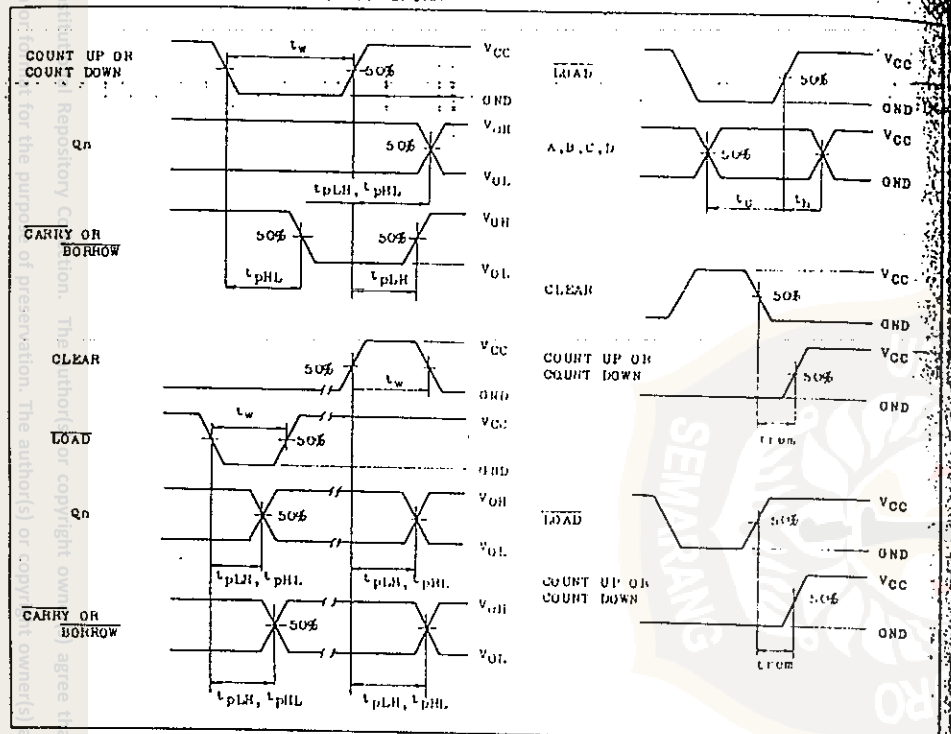
$$I_{DD(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

$I_{CC(opr.)}$ TEST WAVERORM

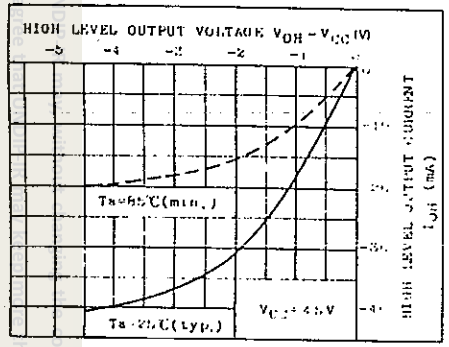


* TRANSITION TIME OF INPUT WAVEFORM IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST.

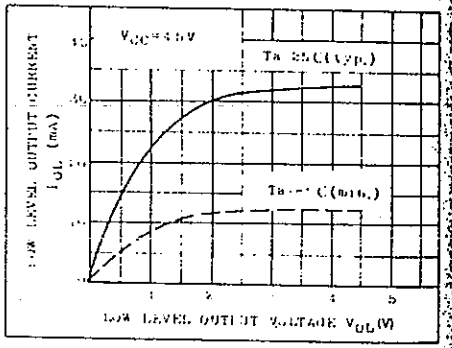
SWITCHING CHARACTERISTICS TEST WAVEFORM



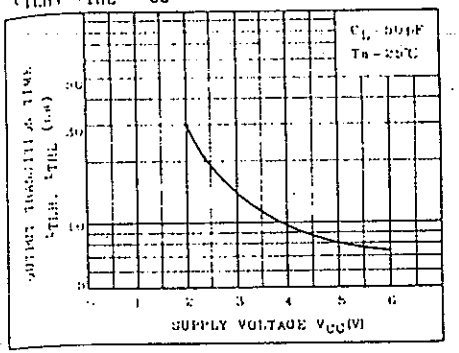
I_{OH} CHARACTERISTICS



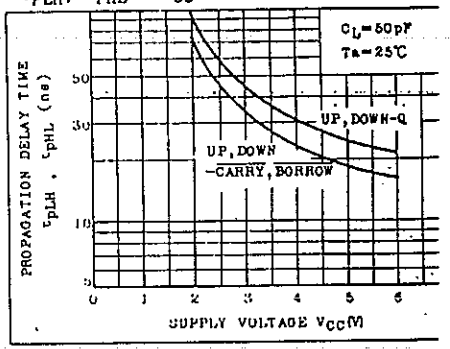
I_{OL} CHARACTERISTICS



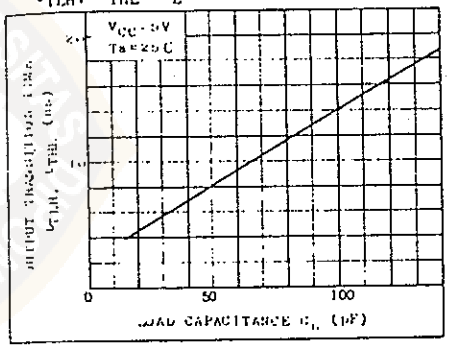
t_{TLH}, t_{THL} - V_{CC} CHARACTERISTICS (TYP.)



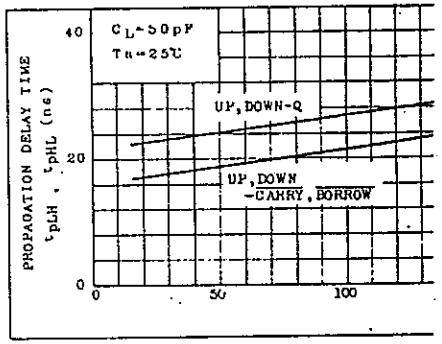
t_{PLH}, t_{PHL} - V_{CC} CHARACTERISTICS (TYP.)



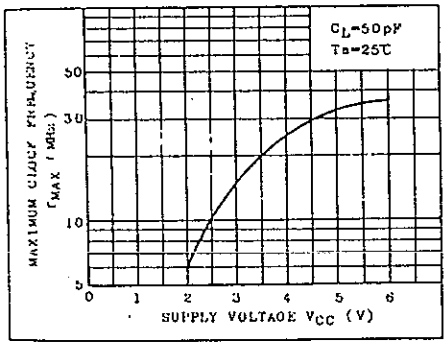
t_{TLH}, t_{THL} - C_L CHARACTERISTICS (TYP.)



t_{PLH}, t_{PHL} - C_L CHARACTERISITCS (TYP.)



f_{MAX} - V_{CC} CHARACTERISTICS (TYP.)



t_w - V_{CC} CHARACTERISTICS (TYP.)