

TIME-DEPENDENT DIELECTRIC BREAKDOWN CHARACTERIZATION OF A HIGH VOLTAGE CAPACITOR

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ABSTRACT

NXP Semiconductors Business Unit (BU) Automotive is a corporate organization that provides design technology for the automotive product creation process.

The assignment for this internship is to create a high voltage Time-dependent Dielectric Breakdown (TDDB) measurements setup for testing the high voltage capacitors inside galvanic isolation. The project starts with designing the schematic, selecting the right component and doing PCB layout for the measurement setup, adapting the software for the automation, and also doing TDDB measurement on the capacitor. From the TDDB measurement, it is expected we will be able to predict the reliability and lifetime of these capacitors. The lifetime of this capacitor is important, due to this product will be applied in car which requires a long lifetime.

From the results of investigating the measurement, breakdown value for negative voltage is smaller than positive voltage. The pads of the package have a sharp point (like a needle) which involved a strong electric field at this point. Tiling and floating metal 3 make the breakdown voltage become smaller. This is because tiling is pieces of metal which reduce the total thickness of inter metal dielectric. Failure analysis shows the damage always happen at the sharp corner, due to sharp electric field in this area. 1,6mm on PCB board wire spacing is too small for high voltage breakdown measurements above 1,6kV.

Keywords : TDDB, capacitor, reliability, failure, lifetime

1. Introduction

1.1. Company Background

NXP BU Automotive is a corporate organization that provides design technology for the automotive product creation process.

The BL Automotive addresses the following markets:

- Networking products. BL Automotive develop a range of standalone transceiver and Active Star products.
- Analog Mixed Signal products in automotive Electronic Control Unit (ECU)'s. BL Automotive addresses this market from their established position in standalone CAN/LIN/FlexRay transceivers.

1.2. Context of Assignment

The assignment for this internship is to create a high voltage Time-dependent Dielectric Breakdown (TDDB) measurements setup for testing the high voltage capacitors inside galvanic isolation. The project starts with designing the schematic, selecting the right component and doing PCB layout for the measurement setup, adapting the software for

the automation, and also doing TDDB measurement on the capacitor. From the TDDB measurement, it is expected we will be able to predict the reliability and lifetime of these capacitors. The lifetime of this capacitor is important, due to this product will be applied in car which requires a long lifetime.

1.3. Limitation

The recommendations in the end of this thesis research are strictly limited determined by characterizing the capacitor only and not the digital isolator.

1.4. Initial Condition

Since NXP has produced the transceiver but do not have digital isolation, so the consumers use the competitor's isolator.

1.5. Description of assignment

In general, the strategies to accomplish the project are described as follows:

1. Literature review

Research is done to study the requirements, literatures, existing applications, and available options for the application development.

2. Package Product Setup

It started with building a prototype with fundamental structure design of the application, to be followed with the final design. To accompany the prototype, documentation about conceptual and technical design development process, analysis, and future recommendations.

3. Wafer level Setup

It started with adapting software of the application, to be followed with the measurement. To accompany the software, documentation about measurement development process, analysis, and future recommendations.

2. Literature Review

2.1. Galvanic isolation

Galvanic isolation provides a barrier between two sections of electrical systems that stops a direct current flowing from one section to the other, while information still can be delivered between the 2 sections. It provides a physical space, i.e. no connection, between the sensor source and the actual equipment.

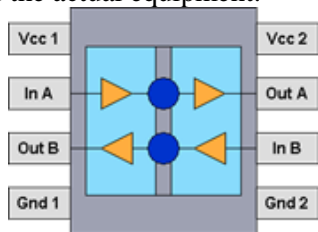


Figure 1 Schematic diagram inside the isolator

2.2. Digital Isolation

Digital isolation is used in automotive to separate the high voltage section to the low voltage section in which contains the control electronics. In case of error in the electric power stage, the control electronics will not be damaged.

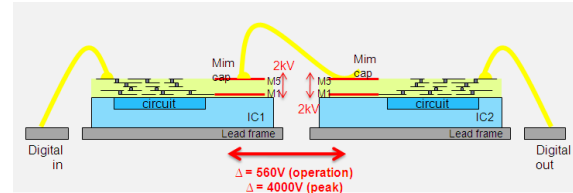


Figure 2 Cross section of isolator

2.3. Silicon on Insulator (SOI) Process

The isolator will be fabricated in an SOI process. SOI is a semiconductor manufacture technique for IC and microchips.

SOI fabrication process :

1. Separation by implantation of Oxygen (SIMOX)

SIMOX is direct injection process of pure oxygen into the silicon wafer at extremely high temperature. The oxygen bonds with the silicon and forms thin layers of silicon oxide. This layer of silicon oxide film is perfect enough that it bonds with the pure crystal silicon layer.

2. Epitaxial growth

A lightly-doped epitaxial layer was grown on top of more heavily doped silicon. Epitaxial layer can be grown to precise doping concentrations, providing better control of the device characteristic.

3. Diffusion of layers

4. Photo lithography

A light-sensitive optical resist is applied onto the wafer. A certain pattern or mask will be defined in the photoresist layer. A light-sensitive film of optical resist is applied onto the wafer. It removes unexposed parts of the photoresist layer.

2.4. Time-dependent dielectric breakdown (TDDB)

Breakdown in oxide is defined as the moment when there is a defect of an oxide layer. TDDB is a failure mode for dielectric materials like silicon dioxide (SiO_2) as it specify the life time of an isolator.

Dielectrics have insulation properties which determined by their physical and chemical composition, including impurities and imperfections. The capacitor dielectric thickness and material type can vary from product to product. It is well understood that this composition can change causing the insulation

properties to change over time and result in the dielectric failure. These changes are accelerated by applying an electric field across the dielectric and/or by increasing its temperature.

3. Package Product Setup

3.1. Implementation

The Device Under Test (DUT) will be put in the DIL Package (or another semiconductor package e.g SO8 or S016). Practically the TDDDB is determined by applying a stress voltage across the isolator, while maintaining the ambient temperature at 150°C.

3.1.1. Hardware

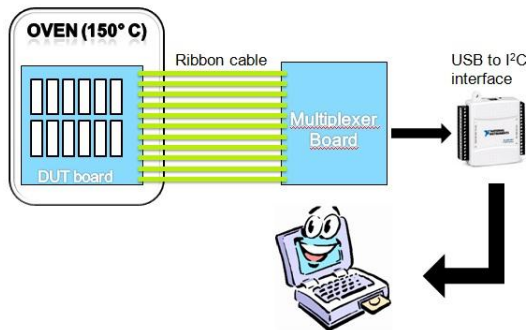


Figure 3 TDDDB measurement setup

The hardware is divided into two parts. DUT board is a high voltage and high temperature board which will be placed inside an oven at 150° Celsius. Multiplexer board is the low power board which is used to monitor the status of the capacitors.

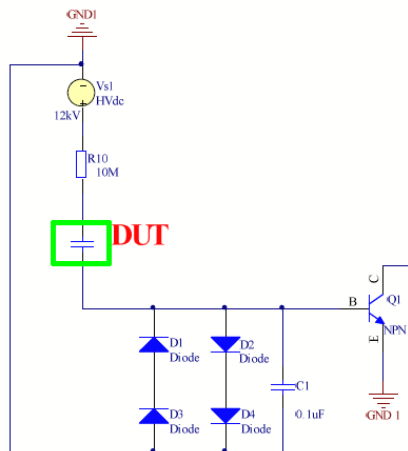


Figure 4 DUT board

As shown in **Error! Reference source not found.**, the DUT board consists of the DUT,

diode, capacitor, transistor, and resistors. The 10MΩ resistor is used to limit the current, maximum 1mA. The diodes will limit the voltage to a maximum of 1.4 volt to the transistor. Two diodes are placed on the opposite polarity because eventually the capacitor will be stressed also using AC voltage. Due to the optocoupler is not be able to detect leakage currents as low as 1nA, a bipolar transistor is used to amplify the leakage current before it goes to the optocoupler.

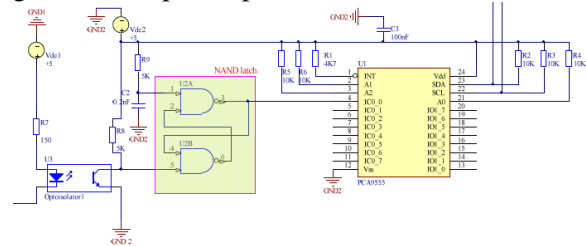


Figure 5 Multiplexer board

The multiplexer board consists of optocoupler, resistors, NAND latch, and PCA9555 as the multiplexer. On the multiplexer board, two power supplies and grounds are separated to protect the transistor and the equipment behind it (i.e computer). The 150Ω resistor is used to limit the current flowing into the optocoupler and the transistor on board 1, based on datasheet the forward DC Current is 40 mA. The 5KΩ resistor is used as a pull-up resistor and also to limit the current flowing into the optocoupler, based on datasheet, the collector saturation voltage is 1,4 mA. The series RC circuit is used to avoid the race conditions on the NAND latch input. The NAND latch is used as one time trigger memory which will be low when the DUT is broken. The PCA9555 serves as an interface between the board and the computer. PCA9555 will read the output of each optocoupler and send the reading to the computer.

On the DUT parallel board, there are 16 DUT and also 16 output channels go through the multiplexer board. On the multiplexer parallel board, there are 16 channels input from the DUT board and 16 output channels go through the PCA9555 as the multiplexer.

On the PCB layout, to avoid flash over between high voltage and low voltage track, the minimum distance between those tracks is 14 mm. As known, the air insulation voltage is ±

1kV/mm. For the high voltage track, only use the top layer to prevent the parasitic capacitance of PCB. Due to the oven size, the requirement size for the DUT board is maximum 35x45 cm.

3.1.2. Software

The readout of the measurement data is done by the computer via multiplexer board and the USB8451 interface. The measurement log contains the time of the breakdown and time to fail for each DUT, The software is written in LabView 2010 and the output file will be saved in an excel format.

3.2. Analysis & report documentation

3.2.1. HV DC Breakdown Measurement on 16-DIL Empty Package

The measurement on the empty package is done to find out that the package will not interfere with the capacitor breakdown measurement and to have a first impression doing a high voltage breakdown measurement. Measurement is divided into two conditions, in air and in vacuum (5.10^{-7} mbar).

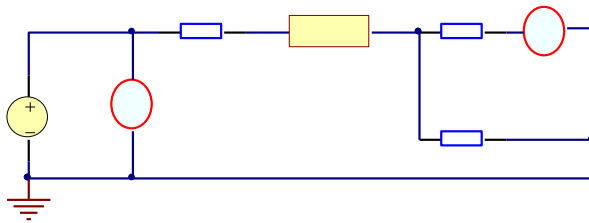


Figure 6 Measurement configuration

Table 1 Result for HV DC breakdown measurement on DIL 16 empty package in air

Pins	Breakdown Value (kV)			
	Positive		Negative	
	1st	2nd	1st	2nd
1 & 8	7,5	7,6	6,3	6,6
2 & 8	7	7,6	6	6
4 & 5	4	4	3,4	3,5
4 & 8	6,3	6,2	5,2	5,1
8 & 9	6,5	6,7	4,8	4,9

Measurement in air shows there is spark between pin 4 & 5 during breakdown, current is limited by the air. Refers to Table 1, breakdown between pins while in air is 1.57 kV/mm.

As shown in Table 1, breakdown value for negative voltage is smaller than positive voltage. The pins of the package have a sharp point (like a needle) which caused a strong electric field at this point. Pins in the air act like anode pole on diode. When positive voltage is applied to the pins, protons occur. Protons are not attracted to pins, because they have the same polarity. When negative voltage is applied to the pins, electrons occur. Electrons are attracted to positive charge on the other pins. When electrons collide with an air molecule on its way to a positive pin it causes ionization. This explains why the negative breakdown value is smaller than positive breakdown value.

For the measurement in vacuum, the current compliance is $1\mu\text{A}$. The measurement in vacuum will measure the internal breakdown of the package.

Table 2 Result for HV DC breakdown measurement on DIL 16 empty package in vacuum

Pins	Distance (mm)	Measured Breakdown Voltage (kV)	Extrapolated Breakdown Voltage (kV/mm)
4 & 5	0.2	15	75
4 & 5	0.2	19	80
1 & 8	0.3	>30	>100
15 & 16	0.4	19	47.5

Measurement in vacuum did not show spark during breakdown. The second measurement between pin 4&5 done as a comparison to previous measurement, it gives almost the same result. As shown in Table 2, there is no breakdown detected between pin 1 & 8. The result of the measurement between pin 15 & 16 was expected to have a higher breakdown value compare to the other pin due to the distance. In practice, it appears to be comparable to the result between pin 4&5. This might indicate that the distance between the pins outside the package is still the limiting factor.

3.2.1. HV DC Breakdown Measurement on other product

Measurement Setup are using power supply 12 kV, resistor 10 M Ω as current limit then the current limit to 1mA, plastic package product, and measurement in air.

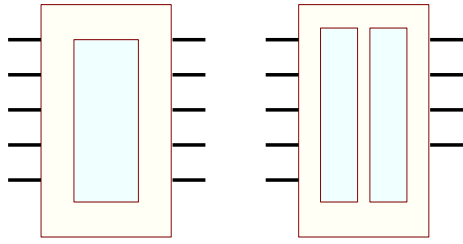


Figure 7 Single and dual die chip

Table 3 Result for HV DC breakdown measurement on competitor product

Product	Breakdown Values			
	Positive		Negative	
	1st	2nd	1st	2nd
Silabs	7,25 kV	-	7,3 kV	-
NXP EZ-HV Single die	730 V	790 V	790 V	790 V
NXP EZ-HV Dual die	750 V	770 V	790 V	810

3.2.1. HV DC Breakdown Measurement on BD3 Module

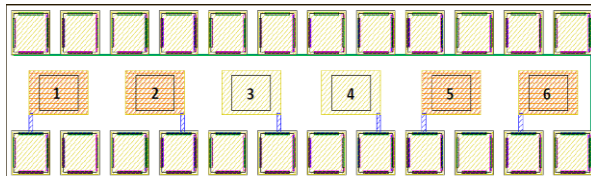


Figure 8 The layout of the module ABCD9_BD3

In this module, a thick oxide is placed rather than M2-M4. There is no M2, M3, and M4, except for structure 5 and structure 6, the floating M3 exist.

Structure 1: This structure is a capacitor between poly-Si and M5. Tiling for all metal levels is present in this structure. Poly-Si is connected to bondpad 1.

Structure 2: This structure is the same as Structure 1, without tiling for all metal. Poly-Si is connected via bondpad 4.

Structure 3: This structure is an M1 to M5 capacitor, thus containing all IMD layers as the dielectric. Tiling for M2, M3 and M4 is present. The M1 electrode is connected to bondpad 6.

Structure 4: This structure is the same as Structure 3, except that 20 μm tile-exclusion rings are added to M2, M3 and M4. M1 connection is via bondpad 8.

Structure 5: This structure is a capacitor between Poly-Si and M5, with a floating M3 plate. Tiling in M2 and M4 is present. M1 is connected to bondpad 9.

Structure 6: This structure is the same as Structure 5, without tiling in M2 and M4. The M1 connection is via bondpad 11.

Table 4 Result for HV DC breakdown measurement on ABCD9 BD3 Module

Structure	Breakdown Values (kV)					
	Positive			Negative		
	1	2	3	1	2	3
Structure 1	1,7	1,8	1,7	1,9	1,8	1,9
Structure 2	3,6	3,7	3,7	3,1	3,6	3,7
Structure 3	1,5	1,5	1,4	1,6	1,6	1,6
Structure 4	3,6	3,9	3,4	3,4	3,4	3,4
Structure 5	1,6	1,6	1,6	1,7	1,8	1,7
Structure 6	2,7	2,7	2,5	2,5	2,5	2,5

From the table above, the good structure are structure 2 (Poly Si - M5 without tiling) and structure 4 (M1 - M5 without tiling). Tiling and floating M3 make the breakdown voltage become smaller, because these are pieces of metal between the electrodes of the capacitor which reduce the remaining thickness of the inter metal dielectric, so the current will flow easily to the other dielectric. Without tiling means dielectric layer will be directly attached to each other. Based on measurement on structure 1 and structure 3, between Poly Silicon and M1 has the deviation breakdown value about 200 volts.

Due to structure 4 is the best structure, breakdown measurements were taken once again and devoted to the structure 4. Failure analysis conducted to determine where the damage occurred.

Table 5 Result for HV DC breakdown measurement on ABCD9 BD3 Module structure 4

Breakdown value	Breakdown Voltage (Kv)
Positive 1	4,4
Positive 2	4
Positive 3	4,3
Positive 4	4,3
Negative 1	3,5
Negative 2	3,5
Negative 3	3,5

As shown in Table 5, the breakdown voltage is higher than the result in Table 4. This is because on the previous measurement, at the same chip measurements done on several structures so there is a possibility of leakage current affects other structure. Failure analysis shows the damage always happen at the sharp corner, due to strong electric field in this area.

4. Wafer Level Setup

4.1. Equipment

4.1.1. Keithley model 4200-SCS system overview

The Model 4200 Semiconductor Characterization System (4200-SCS) is an automated instrument designed that provides I-V, pulsed I-V, and C-V characterization of semiconductor devices and test structures.

4.1.2. Keithley Interactive Test Environment (KITE)

KITE is an application program for characterizing semiconductor devices and materials. KITE is the primary user interface for the Keithley model 4200-SCS. KITE is a tool that facilitates both interactive characterization of an individual device or automated testing of an entire semiconductor wafer. Tests are organized into individual projects, which are managed and executed by KITE.

KITE features include data plotting functions, the ability to append multiple data runs to a given test and plot those data on the same graph, and the addition of test condition information to a graph.

4.1.3. Keithley User Library Tool (KULT)

KULT is a tool used to make and manage libraries. A library is a collection of user modules. User module is a program written with C language functions. User libraries are created to control instrumentation, analyze data, or perform any other system automation task programmatically. Once a user library has been successfully built using KULT, its user modules can be executed using the KITE software tool.

4.1.4. Keithley 2410 Series Source Meters

The Keithley 2410 source meter combines a precise, low-noise, highly stable DC power supply with a low-noise, highly repeatable, high-

impedance multimeter. This meter can produce voltage from 5 μ V up to 1100V and current from 50pA up to 1.05A.

4.2. Implementation

To characterize the dielectric material that is good to be used in the capacitors, thin layer capacitors have been made. These capacitors have a lower breakdown voltage (<1kV) and can be evaluated on wafer level.

The software for measurement at wafer level needs adaptation. The requirements of the software are implementing the software for device to stop at current compliance and control two separate sourcemeters.

The purpose of control two separate sourcemeters is to reach the higher voltage due to the limitations voltage of each sourcemeters is 1100 volt.

4.3. Analysis & report documentation

The breakdown in a ramp test is mostly detected by a sudden increase of the injection current. In general, the average dielectric strength of capacitors decreases when their area increases. This measurement was conducted to test the software which has been adapted. This measurement will measure TDDB between metal to metal of each layer.

To measure on wafer level, a very small probe needle is used. The measurement also depends on the sequence of events which has been set in KITE. Before performing TDDB measurements, always preceded by I-V measurements with a voltage below the breakdown voltage.

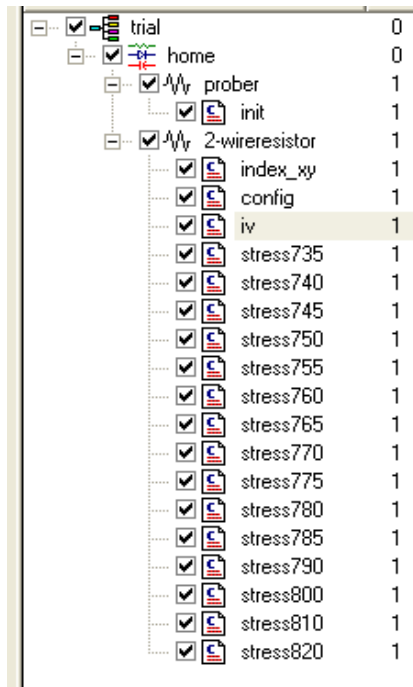


Figure 9 Sequence of events in KITE

As shown in Figure , there are some capacitors which have already breakdown at lower voltage. There are some causes, for example leakage current already occurred, some areas already defected, bad robustness or contamination.

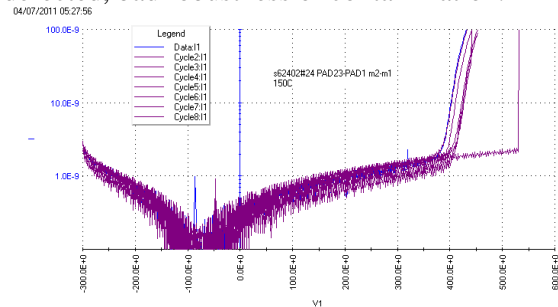


Figure 11 Multi TDDB measurement M2-M1. Maximum time 2ks

As shown in Figure , there is one capacitor which has a breakdown value much higher than the expected value. Usually it can happen because of the bad contact between needle and the wafer. At -100 volt, it appears that some capacitors have leakage currents.

There are large variations in breakdown behavior lifetime over the wafer. The self healing and/or current decrease due to trapping inside the capacitor itself. Self healing happens if the metal withdraws from the corner of the channel probably by surface tension of the molten gate material.

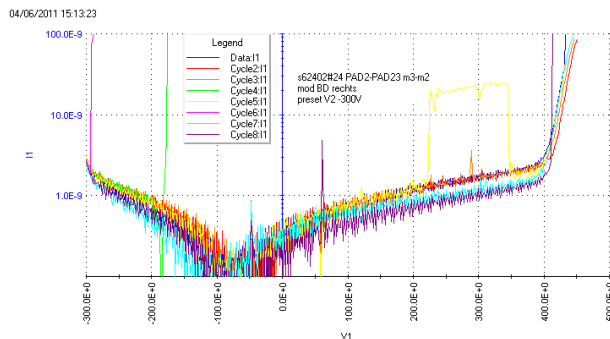


Figure 10 I-V measurement Structure 1 between M3-M2. Temperature 150°C.

To make sure that the software really can control of 2 separate sourcemeters, the different level of voltage is set for each sourcemeters. Sourcemeter 1 on - 300 volt and sourcemeter 2 on 500 volt. From the graph above, the breakdown voltage between metal to metal is ± 700 volt.

As shown in Figure , there is capacitor which has already breakdown in a very low voltage. It is because if one layer breaks down, it becomes conductive such that the electric field in the other layers becomes higher and will subsequently also cause their breakdown.

5. Conclusion and Recommendations

5.1. Conclusion

1. Breakdown value for negative voltage is smaller than positive voltage. The pins of the package have a sharp point (like a needle) which causes a strong electric field at this point.
2. The empty package will not interfere with the capacitor breakdown measurement due to the breakdown value is higher than we needed for capacitor.
3. Tiling and floating M3 make the breakdown voltage become smaller. This is because tiling is pieces of metal which reduce the total thickness of inter metal dielectric.
4. Failure analysis shows the damage always happen at the sharp corner, due to strong electric field in this area.

5. 1,6mm wire spacing is too small for high voltage breakdown measurements above 1,6kV.

5.2. Recommendation

1. Redesign the capacitor with a soft corner will make the breakdown value higher than sharp corner.
2. Check the datasheet of each component if the DUT will be tested in the environment temperature more than 150 degrees Celsius.
3. Measuring an empty package breakdown in isolating oil is a suitable alternative for measuring in a vacuum.
4. Either adjacent pins of the test device have to be straightened, in the high voltage board needs a redesign to avoid arching between adjacent wires.
5. Redesign the wiring diagram or use the 24 DIL package to ensure that any structure placed by skipping a single pin.

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BIODATA



Brechia Nurastu Sasongko, lahir di Banjarnegara, 21 Desember 1988. Telah menyelesaikan studi di Fontys University of Applied Sciences Eindhoven. Saat ini masih menyelesaikan studi Strata-1 di Jurusan Teknik Elektro Universitas Diponegoro

Semarang dengan mengambil konsentrasi Ketenagaan.

Menyetujui dan Mengesahkan,
Pembimbing I

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